

# Bolt Schematic

## Whiskey Lake

2018/12/13

REV : A00

*DY : None Installed*  
*UMA: UMA only installed*  
*OPS: DISCRTE OPTIMUS installed*  
*TypeC: CCG4*  
*TypeC\_5V\_OUT: provide external device power 5V*  
*TypeC\_PWR\_IN: Provide system power via typeC connector.*  
*8111H:Reltek LAN RTL811H*  
*81106E:Reltek LAN RTL8106E*

<Core Design>



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
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Document Number

**BOLT WHL**

Rev

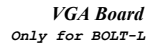
**A00**


Date: Thursday, December 27, 2018

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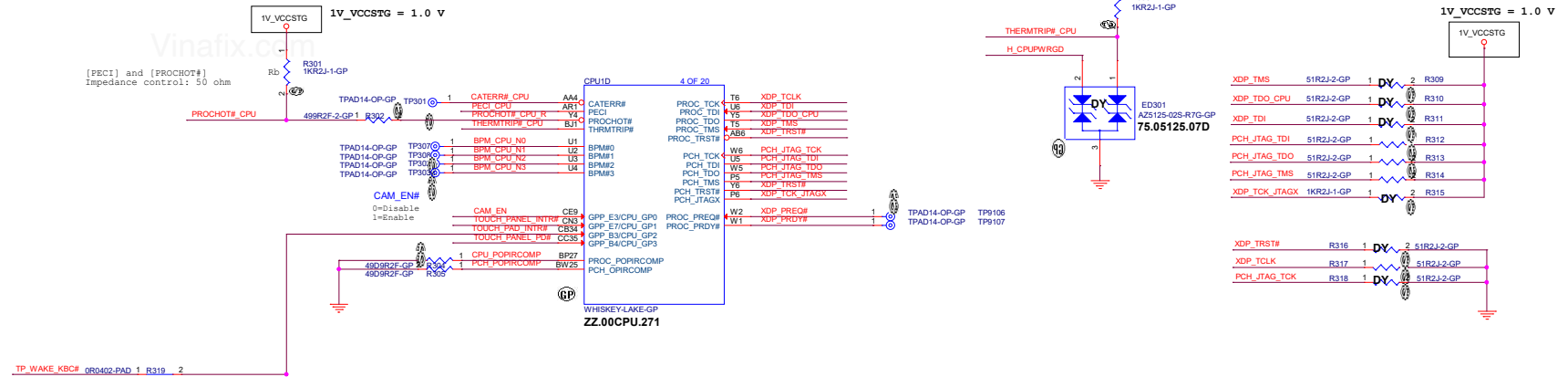
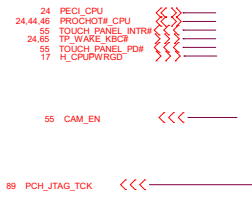
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*Intel CPU*

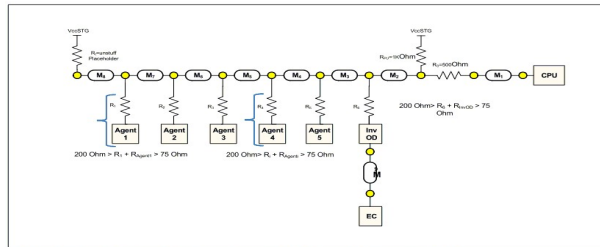


<Core Design>		<b>Wistron Corporation</b> 21F, 8th St., Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		<b>Block Diagram</b>	
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**Main FUNC = CPU**



(#575412) PROCHOT# Routing Guidelines



**Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)**

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254		254	
Topology Guidelines							
Platform resistors values		Rpu = 1KQ, Rs = 500Q, Ri + Ragent = 75-200Q, R6 + Rinvod = 75-200Q					
Platform resistors tolerances		± 5%					

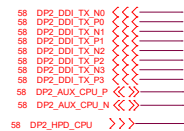
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# Main FUNC = CPU

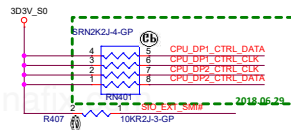
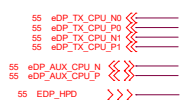
## HDMI 1.4B



## TO DP MUX



## EDP



### 5.2.7 Compensation Signal Routing Guidelines

Signal	Trace Width	Termination	Resistor Value	Max Length
eDP_RCOMP	1.0mm	Series	200Ω ±1%	100mm

### 5.2.8 eDP Disabling and Termination Guidelines

Signal	Trace Width	Termination	Resistor Value	Max Length
eDP_RCOMP	1.0mm	Series	200Ω ±1%	100mm

### (#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-kΩ resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-kΩ resistor	NC

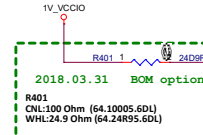
Table 9-1. Pin Straps (Sheet 3 of 4)

#566439

Signal	Usage	When Sampled	Comment
SP10_I03	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2SD_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. <b>Notes:</b> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. <b>Notes:</b> 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. <b>Notes:</b> 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. <b>Notes:</b> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. <b>Notes:</b> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F6 / CNV_RST_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNV1 enable. 1 = Integrated CNV1 disable.

## HDMI 1.4B

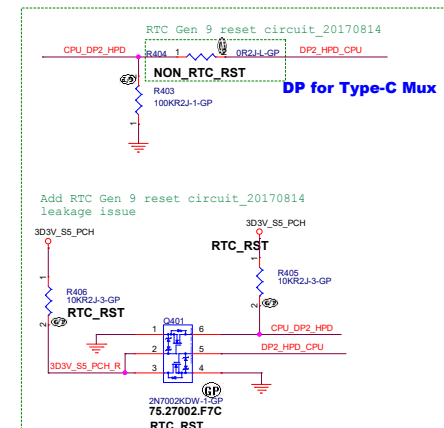
## TO DP MUX



Pin Straps (Sheet 4 of 4)

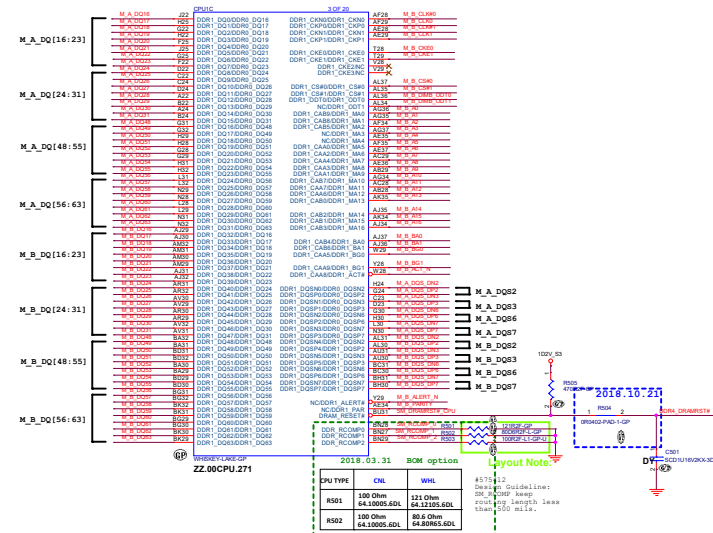
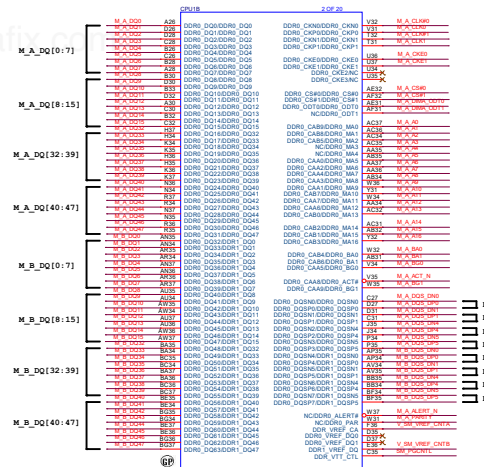
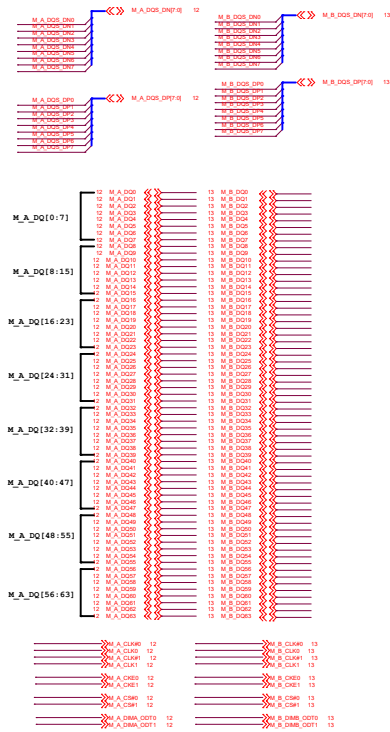
#566439

Signal	Usage	When Sampled	Comment
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% <b>Note:</b> This strap should only be used for specific targeted 1S battery systems.
GP07	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. <b>Warning:</b> This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)

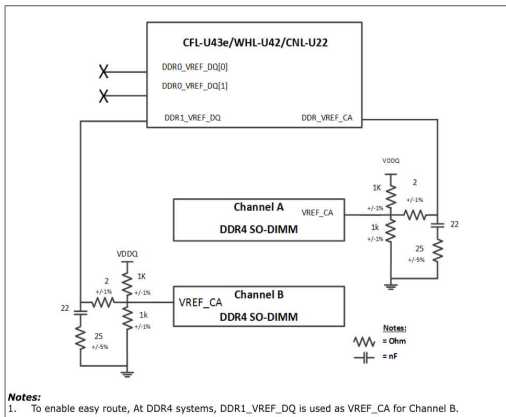




DDR4 ball type: Non-Interleaved Type



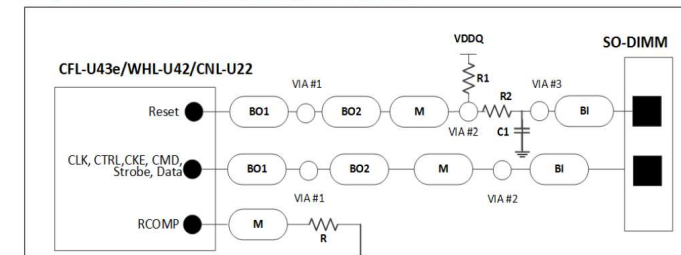
**Figure 4-1. WHL U DDR4 SODIMM V<sub>REF-CA</sub> Overview**



**Notes:**

1. To enable easy route, At DDR4 systems, DDR1\_VREF\_DQ is used as VREF\_CA for Channel B

## WHL U DDR4 SODIMM T3/8L Signals Topologies



**Note:** DRAM\_RST C1 capacitor should not be installed

RCOMP (0/1/2)	M	US/SL	500			15	20	25	CFL-U43e/ WHL-U42; 121/80.6/ 100  CNI-U22; 100/100/ 100
Reset	BO1	US	500	8000		3		6	R1=470 [5%] R2=0 C1=0.1uF (no stuff)
	BO2	SL	800-BO1			3.5		12	
	M	SL			50	4		20	
	BI	US				4		20	

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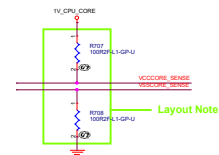
Diagram illustrating the SVID Data, SVID Clock, and SVID Alert signals.

**SVID DATA:** The signal path starts with RTD1 (pin 1) connected to the CPU. The signal is labeled "SVID DATA\_CPU\_R". The signal is then connected to the "RTD8 100RUF-L1-GP-U" block. The signal is labeled "SVID\_DATA\_CPU".

**SVID CLOCK:** The signal path starts with RTD2 (pin 2) connected to the CPU. The signal is labeled "SVID\_CLK\_CPU\_R". The signal is then connected to the "RTD5 100RUF-L1-GP" block. The signal is labeled "SVID\_CLK\_CPU".

**SVID ALERT:** The signal path starts with RTD3 (pin 3) connected to the CPU. The signal is labeled "SVID\_ALERT\_CPU\_R". The signal is then connected to the "RTD4 100RUF-L1-GP" block. The signal is labeled "SVID\_ALERT\_CPU".

The diagram also includes a date stamp "2018.10.21".



SVID Signals	VDSOUT=100Ω, VIDSALERT#
VDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock

#575412

IMV/P8/P9 Controller

Vss\_SENSE

Voc\_SENSE

R1

Vss Plane

Voc Plane

R2

R1-R2 100 ohm catch resistors

Die

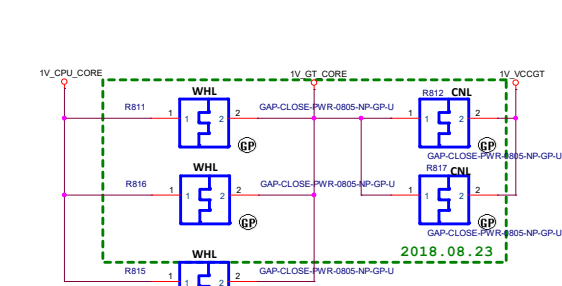
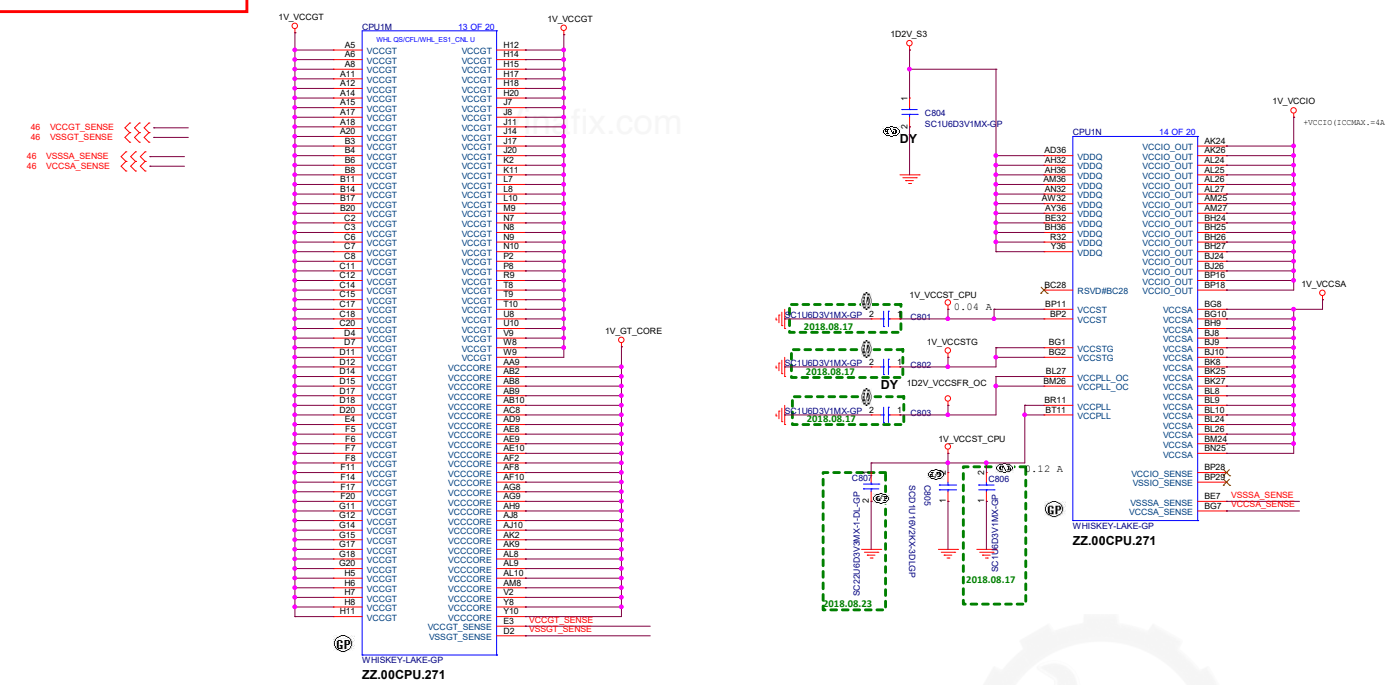
Processor Package

Socket

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
Vcc <sub>GT</sub> _SENSE / Vss <sub>GT</sub> _SENSE			
Vcc <sub>SA</sub> _SENSE / Vss <sub>SA</sub> _SENSE			
Vcc <sub>IO</sub> _SENSE / Vss <sub>IO</sub> _SENSE <sup>[1]</sup>		NA	

- R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc\_SENSE/Vss\_SENSE line resistance.

Main FUNC = CPU



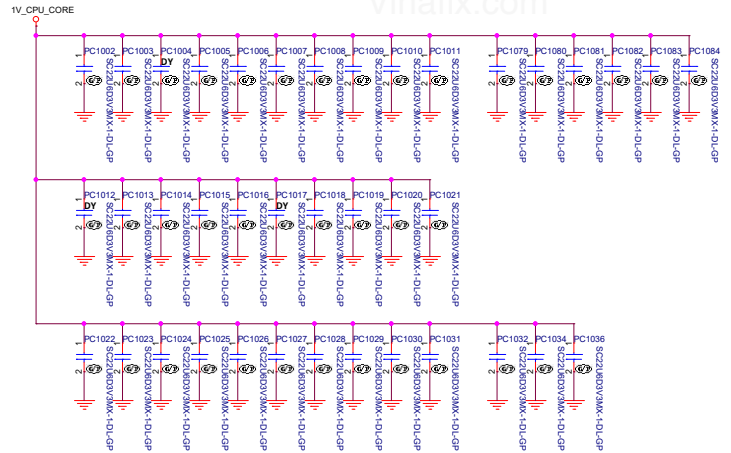
Design Target	CPU support	GP	Stiffing options for compatibility	Incremental VR BOM vs KBL	Incremental board area vs. KBL
Cost optimized entry design (C13 SMBO-ICP)	CNL only		None	No increase expected for CNL vs. KBL U22	~0mm² vs. KBL U22
Premium design (C17-C13)	WHL only		None	Load line change anticipated to drive incremental cost vs. KBL R	TBD
Scalable mainstream design (C17-ICP)	WHL and CNL		Jumpers vary by SKU: 3 if WHL 1 if CNL	Load line change on WHL anticipated to drive incremental cost vs. KBL R No increase expected for CNL vs. KBL U22	TBD

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



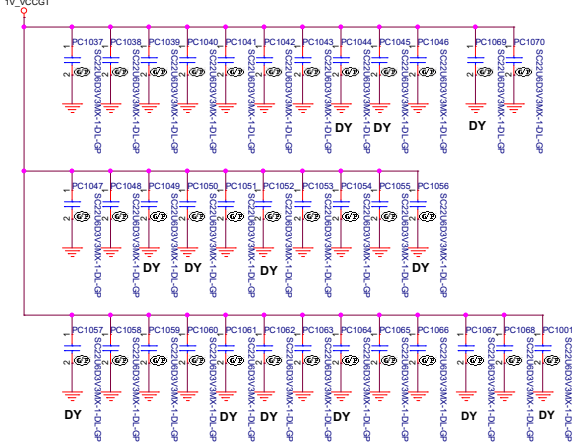
# 1V\_CPU\_CORE

22U 0603 x 39 (3DY)



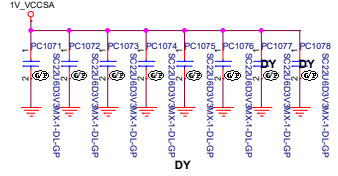
# VCCGT

22U 0603 x 35 (3 DY)



# VCCSA

22U 0603 x 8 (3DY)



## KBL-R U42 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR) 1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
VDDQ Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCIO Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
VCCPLL Power Plane at V1P0A VR output	1x 0.1uF 0402	Placed at primary side near to VR output

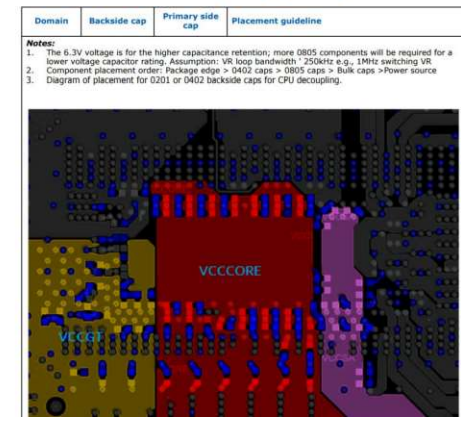
**Notes:**

- These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

## KBL-R U42 Decoupling Requirements (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	26x 1 uF 0402 or 0201		Refer to diagram in Note 3 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
VCCGT	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
VCCSA	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
VCCIO		4x 1 uF 0402	Place as close to the package as possible
VDDQ		4x 10 uF 0402	Place as close to the package as possible
VDDQ		3 x 22 uF 0603	Place as close to the package as possible
VDDQ		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQ pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQ BGA routing should not exceed 48mm (RdC). RVP design uses trace L=450um, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
VCCPLL		1x 1 uF 0402	Place as close to the package as possible.
VCCPLL_DC		1x 1 uF 0201	Do not route VCCPLL, VCCPLL_DC, VCCGT closest adjacent layer over any power net other than ground.
VCCGT		1x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

## KBL-R U42 Decoupling Requirements (Sheet 2 of 2)

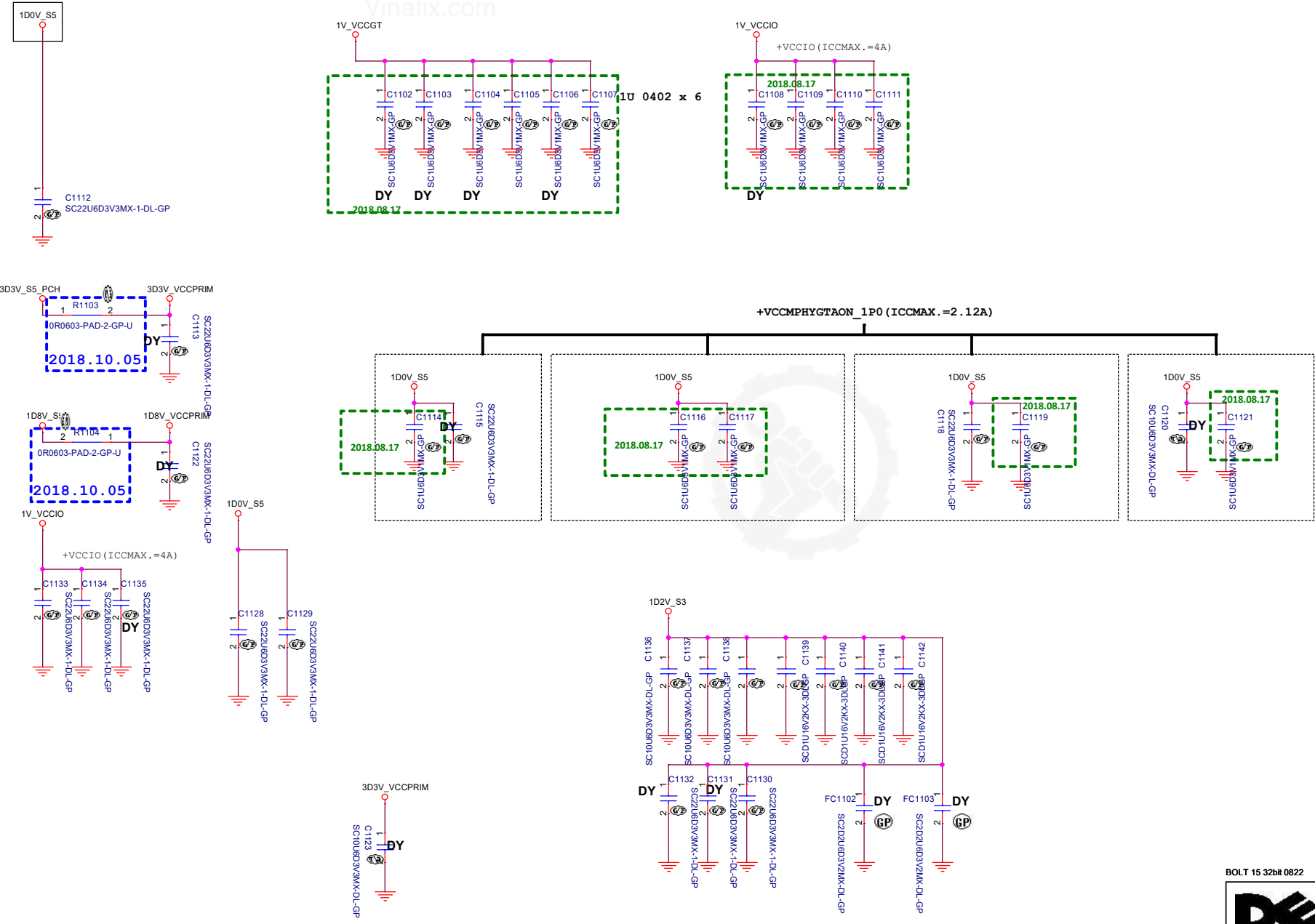


Core Design



Main FUNC = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO



**Layout Note:**

1uF:  
C1174 near N15  
C1180 near K15  
C1173 near AF20  
C1172 near N18  
C1175 near AB19  
22uF :  
C1182 C1184 near N15  
10uF:  
C1176 near N15








(Blanking)

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Title <b>(Reserved)_SODIMM _SODIMM4</b>		
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Date: Thursday, December 27, 2018		Sheet 14 of 106

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GPP_B18 / GSP10_MOSI	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "No Reboot" mode. (Default)</p> <p>1 = <b>Enable</b> "No Reboot" mode (PCH will disable the TCO timer system reboot feature). This function is useful when running ITP/XDP.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PCH_PWROK is high.</li> <li>This signal is in the primary well.</li> </ol>
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GPP\_B18



GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)</p> <p>1 = <b>Enable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>
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GPP\_C2



GPP_CS / SMDALERT#	eSPI or LPC	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>LPC</b> is selected (for EC). (Default)</p> <p>1 = <b>eSPI</b> is selected (for EC).</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol> <p><b>Warning:</b> If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' (eSPI is disabled).</p>
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GPP\_CS



SP10_MOSI	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
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SP10\_MOSI



GPP_D12 / ISH_SPI_MOSI / GSP12_MOSI	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
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GPP\_D12



SP10_I02	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
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SP10\_I02



SP10_I03	Reserved	Rising edge of RSMRST#	<p>External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
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SP10\_I03



HDA_SDO / I2SD0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Enable</b> security measures defined in the Flash Descriptor. (Default)</p> <p>1 = <b>Disable</b> Flash Descriptor Security (guarded). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after PCH_PWROK is high.</li> <li>This signal is in the primary well.</li> </ol>
---------------------	------------------------------------	--------------------------	---

HDA\_SDO / I2SD0\_TXD



GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.</p> <p>0 = 38.4 MHz XTAL frequency selected. (Default)</p> <p>1 = 24MHz XTAL frequency selected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>
---------	-----------------------	------------------------	---

GPP\_H21



GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	<p>An external pull-up or pull-down is required.</p> <p>0 = Integrated CNV enable.</p> <p>1 = Integrated CNV disable.</p>
---------------------	---------------------	------------------------	---

GPP\_F6 / CNV\_RGI\_DT



INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	<p>External pull-up or pull-down is required</p> <p>0 = 3.3V supply is 3.3V +/- 5%</p> <p>1 = 3.3V supply is 3.0V +/- 5%</p> <p><b>Note:</b> This strap should only be used for specific targeted 1S battery systems.</p>
------------	-------------	--	---

INPUT3VSEL



GPD7	Reserved	Rising edge of DSW_PWROK	<p>External pull-up is required. Recommend 100K.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>
------	----------	--------------------------	--

GPD7



GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = Master Attached Flash Sharing (MAFS) enabled (Default)</p> <p>1 = Slave Attached Flash Sharing (SAFS) enabled.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol> <p><b>Warning:</b> This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC Strap is configured to '0' (eSPI is disabled).</p>
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GPP\_H23



NAME	ONLY PROCESSOR, SERIAL, REMOTE (GPP STRAPS)
SPRST	0 = eSPI Flash Sharing Mode (SAFS) enabled (Default)
SPRST	1 = eSPI Flash Sharing Mode (SAFS) disabled

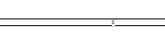
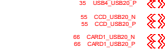
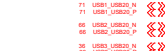
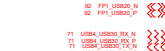
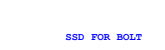
PCH strap pin:



NAME	ONLY PROCESSOR, SERIAL, REMOTE (GPP STRAPS)
SPRST	0 = eSPI Flash Sharing Mode (SAFS) enabled (Default)
SPRST	1 = eSPI Flash Sharing Mode (SAFS) disabled

PCH strap pin:





#543016:  
220 nF nominal capacitors are recommended for Gen 3.  
100 nF nominal capacitors are recommended for Gen 2.

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2018.08.16

2018.08.02

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16
High Speed I/O (HSIO) Type and Lane	PCIe #1	PCIe #2	PCIe #3	PCIe #4	PCIe #5	PCIe #6	GbE	GbE	GbE	SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2	
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes

#### 6.4.1 PCH PCI Express\* Device Down Guidelines

Figure 6-3. PCH PCI Express\* Device Down at 2.5, 5, and 8 GT/s Topology

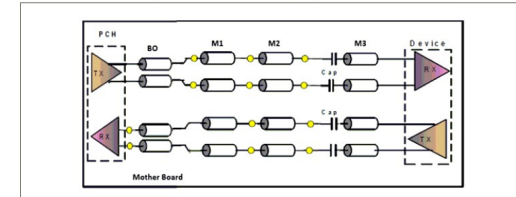


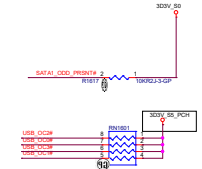
Table 6-6. PCH PCI Express\* Device Down Routing Guidelines (Sheet 1 of 2)

Parameter	Segment	Stack-up (MS/SL/DSL)	Units	2.5 GT/s Routing	5 GT/s Routing	8 GT/s Routing
Reference Plane	BO, M1, M2, M3	MS/SL/DSL	NA	GND	GND	GND
Break-Out Max Length	BO	MS/SL/DSL	mm(mils)	15.2(598.42)	15.2(598.42)	15.2(598.42)
Post-AC Capacitor Max Length	M3	MS	mm(mils)	8(314.96)	8(314.96)	8(314.96)

#543659: The xHCI controller supports USB Debug port on all USB3.0 capable ports.

USB 2.0 Table

Pair	Device
1	USB1 (USB Charger)
2	IO board USB2.0
3	USB2 CON
4	TYPE-C USB/ I2C MIX
5	Finger Print
6	CAMERA
7	Card Reader
8	WLAN
9	Touch Panel
10	WLAN (BT)



#### Overcurrent Protection #575412

Whiskey Lake PCH has implemented programmable USB overcurrent signals. The 4 overcurrent pins are to be shared across the USB 2.0 ports and USB 3.1 ports. This allows the platform designer flexibility in routing of the OC pins and allows for unused pins to be configured as GPIOs.

It is the responsibility of system software (BIOS) to program the overcurrent registers of the given USB controller correctly and to make sure that each USB port is protected by only one overcurrent pin. Operation with more than one overcurrent pin mapped to a port is undefined.



#575412  
USB ID and USB0\_SSRX signals are not needed for USB Type-C implementation with Type-C Port Controller (TPC).

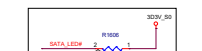


Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

	LP3 DDR_RCOMP	DORA SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIe_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 2000 ±1% on pkg to VSS DDR_RCOMP[1]: 80.60 ±1% on pkg to VSS DDR_RCOMP[2]: 1620 ±1% on pkg to VSS	DDR_RCOMP[0]: 1210 ±1% on pkg to VSS DDR_RCOMP[1]: 80.60 ±1% on pkg to VSS DDR_RCOMP[2]: 1000 ±1% on pkg to VSS	24.90 ±1% to VCCO	49.90 ±1% to GND	100Ω ±1% Differential	118Ω ±1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	X	X				
HDMI			X			
DP			X			
eDP			X			
CFG				X		
PCIe					X	
USB2						X

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```

25.91 SPI_CLK_CPU <<<
25.91 SPI_SQ_CPU >>>
15.25.91 SPI_SI_CPU <<<
15.25 SPI_WP_CPU <<<
15.25 SPI_HOLD_CPU <<<
25 SPI_CS_CPU_N0 <<<
25 SPI_CS_CPU_N1 <<<
01 SPI_CS_CPU_N2 <<<
01 TPM_SPI_ROW >>>

```

PCH\_SMBDATA <<>>  
PCH\_SMBCLK <<>>

SML1\_SMBCLK <<>

SML1\_SMBDATA <<>

CPU\_N\_4 >>>

CLK\_CPU\_P <<<

```
CLK_CPU_P <==
```

```
4_PCIE_CLK_N    >>>
```

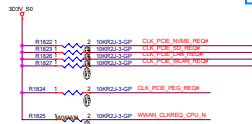
```

I_CLK_CPU_P <==

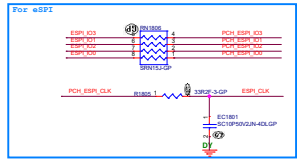
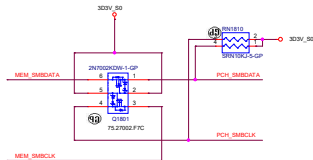
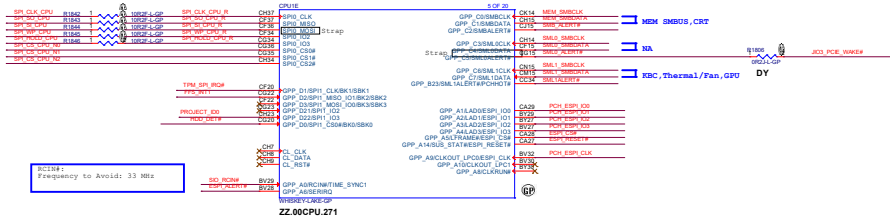
```

### FREE FALL SENSOR

15 SMB\_ALERT# >>>



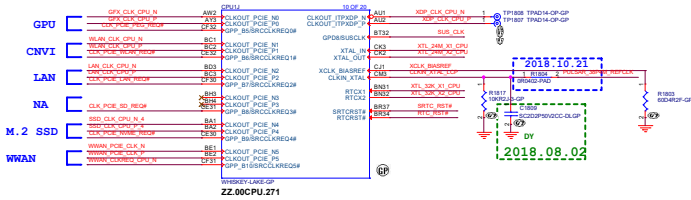
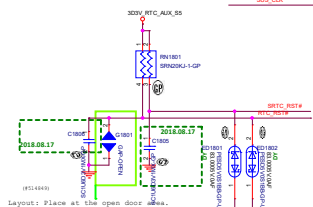
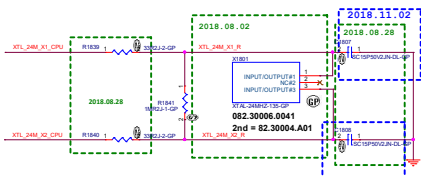
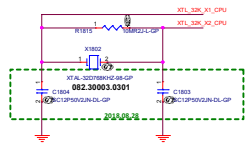
R1842/R1843/R1844/R1845/R1846		
CPU TYPE	CNL(16M+BM)	WHL(16M)
Bolt-L(TPM)	64.10R05.GDL	63.5R134.1DL
Bolt (non TPM)	63.5R134.1DL	64.49R95.GDL



ESPI_Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

<b>eSPI or LPC</b>	Sampled at rising edge of RSMRST#
<b>SML0ALERT# / GPP_C5</b>	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

Signal	Usage	When Sampled	Comment
			<p>This signal has a weak internal Pull-down.</p> <p>This pin determines the destination of access to the BIOS memory array. Also controls the BIOS Boot ROMs destination of (Boot, Segment, Function, other BIOS, etc.)</p> <div style="border: 1px solid black; padding: 5px; margin: 10px 0;"> <p><b>Bit 6</b>      <b>BIOS Destination</b></p> <p>0      <b>SPU (Default)</b></p> <p>1      <b>LC</b></p> </div> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal Pull-down is disabled after P1TEST# = 1.</li> <li>If option 1 (LC) is selected, all pull-up and pull-downs will be placed on LC, but all pull-downs are disabled on SPU.</li> <li>If option 2 (SPU) is selected, all pull-up and pull-downs will be placed with a weak selected in order to bias the signal to SPU.</li> <li>BIOS Destination will be selected by the BIOS boot ROMs using or using BIOS Destination bit will not affect other accesses initiated by user I/O.</li> <li>Integrated GPU is selected.</li> <li>This signal is in the primary pull.</li> </ol>
GPSP1_M0SE/ GPSP1_S02		BIOS Boot ROMs group 1 BIOS	<p>Rising edge of PCH_P0SEL#</p>
			<p>This signal has a weak internal Pull-down.</p> <p>— <b>LC</b> is selected for (C). (Default)</p> <p>— <b>SPU</b> is selected for (S).</p>
UNALALERT/ GPV_CS		BIOS Boot ROMs group 1 BIOS	<p>Rising edge of RSTB#</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal Pull-down is disabled after RSTB# = 1.</li> <li>This signal is in the primary pull.</li> </ol>



CLKIN_XTAL	I		<b>XTAL Clock Input:</b> Single ended integrated CNV (Connectivity) XTAL clock input
------------	---	--	--

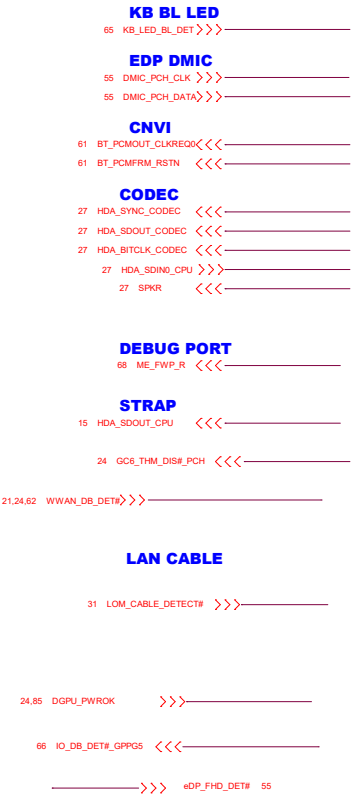
Group	Signal Name	Description
System Management	INTRUDER#	Intruder Detect: This signal can be set to disable system if box detected open.
RTC	SRTCRST#	Secondary RTC Reset: This signal resets the manageability register bits in the RTC well when the RTC battery is removed.
RTC	RTCRST#	RTC Reset: When asserted, this signal resets register bits in the RTC well.

The diagram shows the signal path for XCLK\_BIASREF. It starts at the PCH block, goes through multiplexer M1, then a resistor R1, then multiplexer M2, and finally to ground.

Parameter	Segment	Stack-up	Rule
Reference Plane	M1, M2	MS/SL/DSL	Ground
Single Ended Trace Impedance	M1, M2	MS/SL/DSL	Refer Note
Max Total Length	M1+M2	MS/SL/DSL	1000mils(25.4mm)
Resistor (R1)			60 Ohm $\pm$ 1.0%
Max Transition Via Count			2



Main Func = PCH



Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.

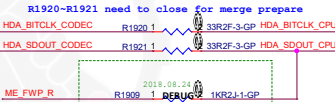
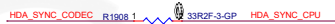
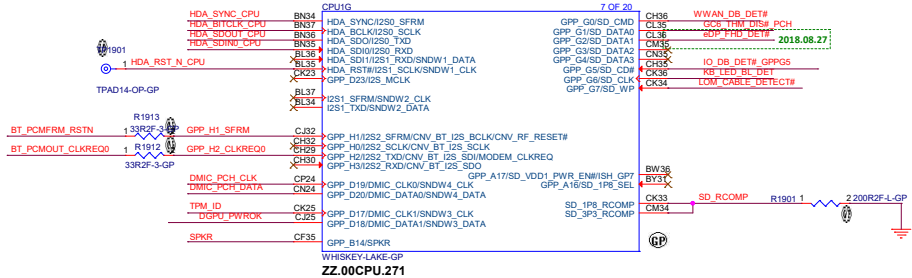
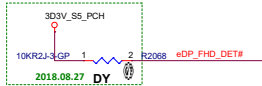
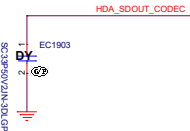
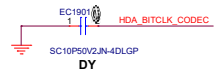
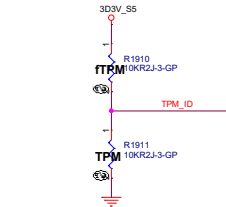
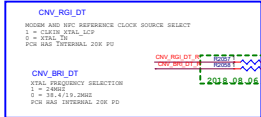
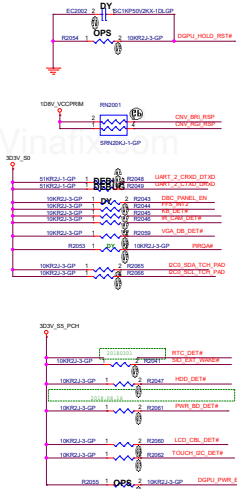
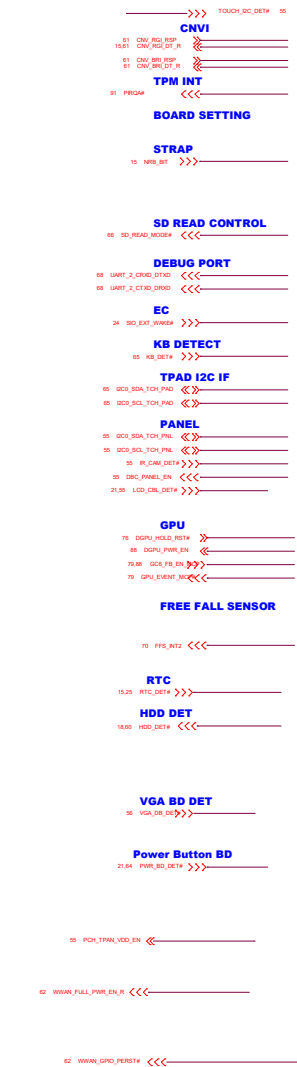


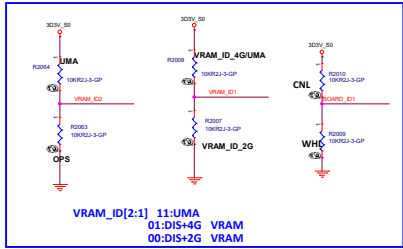
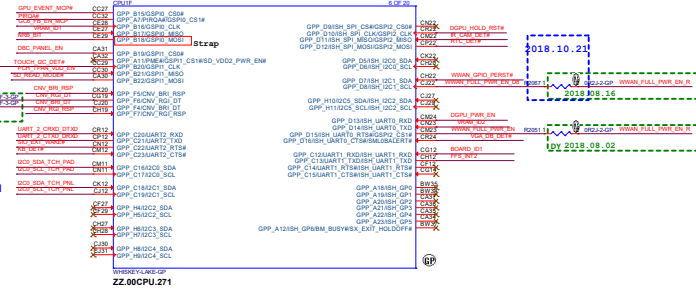
Figure 3-2. RCOMP Recommendation for WHL U42 and CFL U43e - Part 2

	SD_RCOMP_1P8	SD_RCOMP_3P3	EMMC_RCOMP	XCLK_BIASREF	CNV_WT_RCOMP	PCH_OPIRCOMP	PROC_POPIRCOMP
Board Rterm (ohm)	200Ω +/-1% to GND	200Ω +/-1% to GND	200Ω +/-1% to GND	60Ω +/-1% to GND	150Ω +/-1% to GND	49.9Ω +/-1% to GND	49.9Ω +/-1% to GND
Notes: SD_RCOMP_1P8, SD_RCOMP_3P3 and EMMC_RCOMP can be merged into one 200Ω +/-1% to GND resistor. Routing each of them to individual 200Ω +/-1% to GND resistor is an option too.							
Board Rdc (ohm)	<0.1	<0.1	<0.1	<0.5	<0.5	<0.2	<0.2
SD3	X	X					
EMMC			X				
POPI						X	X
XTAL				X			
CNVi_DPHY					X		

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TPAD  
Touch panel



17.4.1 Configurable GPIO Voltage

Except for all pads in GPIO F group and GPD group, all other GPIO pads support per-pad configurable voltage, which allows control selection of 1.8V or 3.3V for each pad. The configuration is done via soft straps.

Before soft straps are loaded, the default voltage of each pin depends on its default as input or output.

- Input: 1.8V level with 3.3V tolerant.
- Output: defaults to '0', except for the following GPIOs which defaults to '1' via a ~20K pull-up to 3.3V:
  - GPP\_B0
  - GPP\_B1
  - GPP\_B11 / EXT\_PWR\_GATE#
  - GPP\_B12 / SLP\_S0#
  - GPP\_H18 / CPU\_C10\_GATE#

A 1.8V device connected to these GPIOs must be capable of taking 20K pull-up to 3.3V.

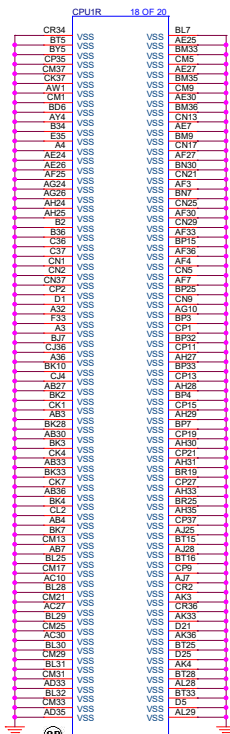
**Warning:** GPIO pad voltage configuration must be set correctly depending on device connected to it; otherwise, damage to the PCH or the device may occur.

- Notes:**
  - GPIO F group supports 1.8V only.
  - GPD group supports 3.3V only.

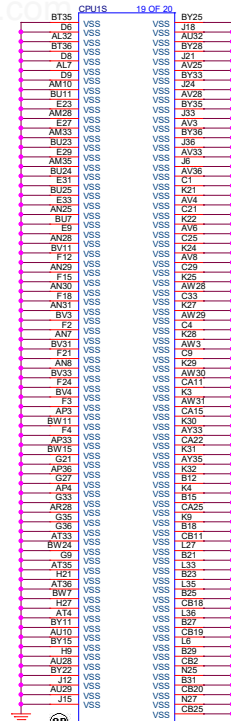




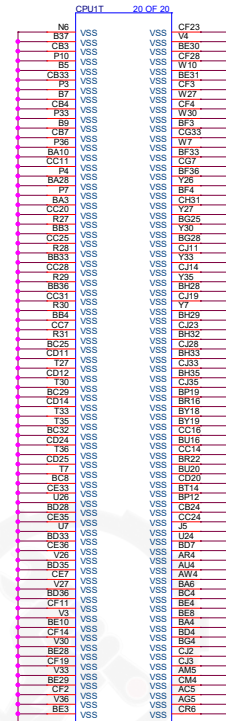
**Main Func = CPU**



WHISKEY-LAKE-GP  
ZZ.00CPU.271

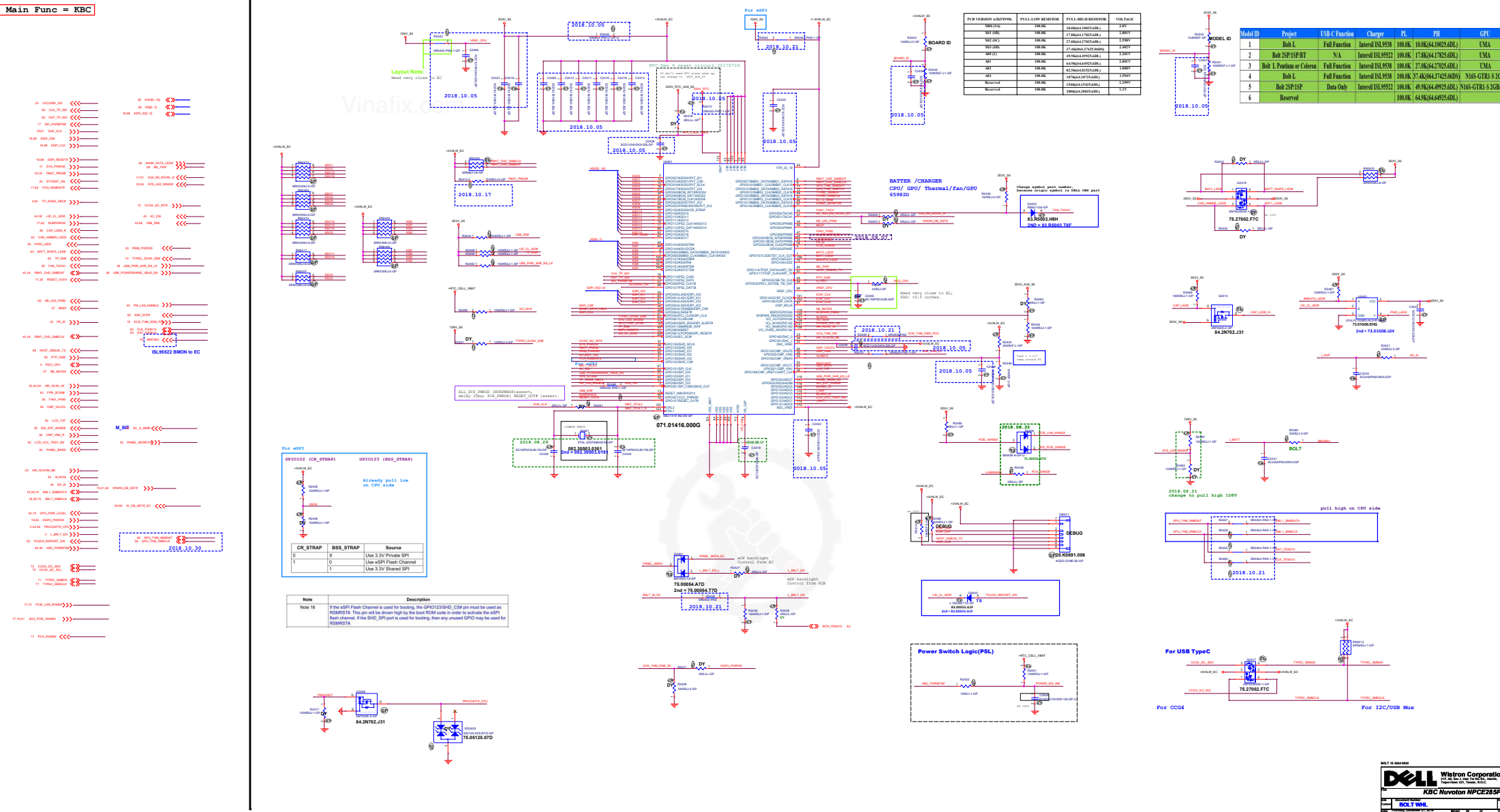


WHISKEY-LAKE-GP  
ZZ.00CPU.271



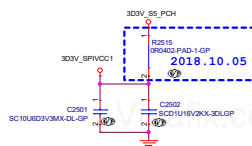
WHISKEY-LAKE-GP  
ZZ.00CPU.271

Main Func = KBC

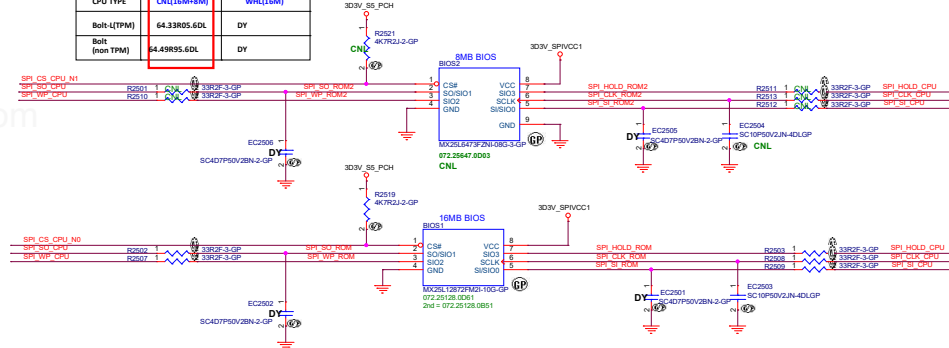


## Main Func = SPI Flash

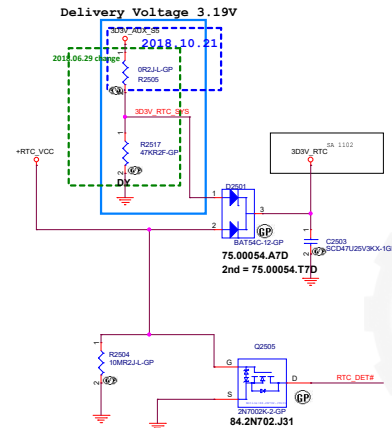
18 SPI\_CS\_CPU\_N1 >>>  
18 SPI\_CS\_CPU\_N0 >>>  
15,18 SPI\_HOLD\_CPU <<<  
24 RTORST\_ON <<<  
53 3V\_SV\_DSW\_OK <<<  
18,91 SPI\_S0\_CPU <<<  
15,18 SPI\_CLK\_CPU <<<  
15,18,91 SPI\_S1\_CPU <<<  
15,20 RTC\_DET# <<<  
24 VCCDSW\_ON <<<  
17,40,45 3V\_SV\_POK <<<



R2502/R2507/R2503/R2508/R2509			
CPU TYPE	CNL(16M+8M)	WHL(16M)	
Bolt-(TPM)	64.33R05.6DL	64.49R95.6DL	
Bolt (non TPM)	064.49R95.56D1	63.R0034.L0L	

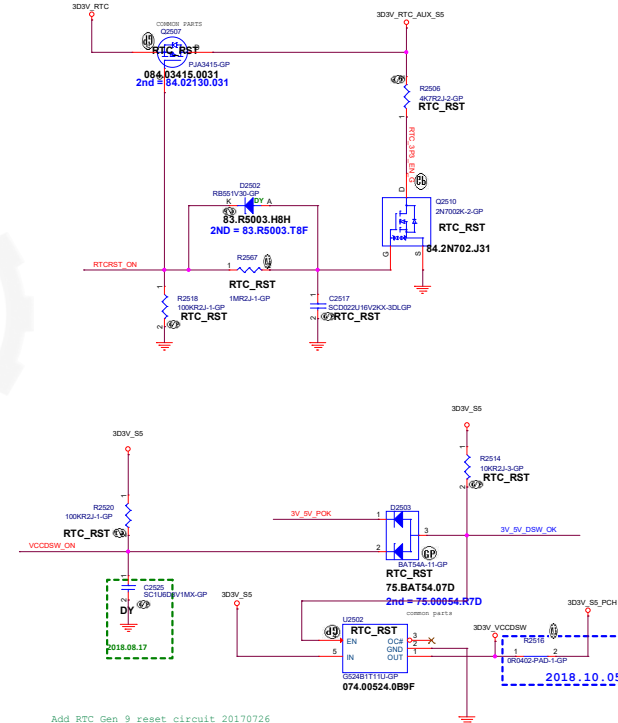


## Main Func = RTC



### 29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW\_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



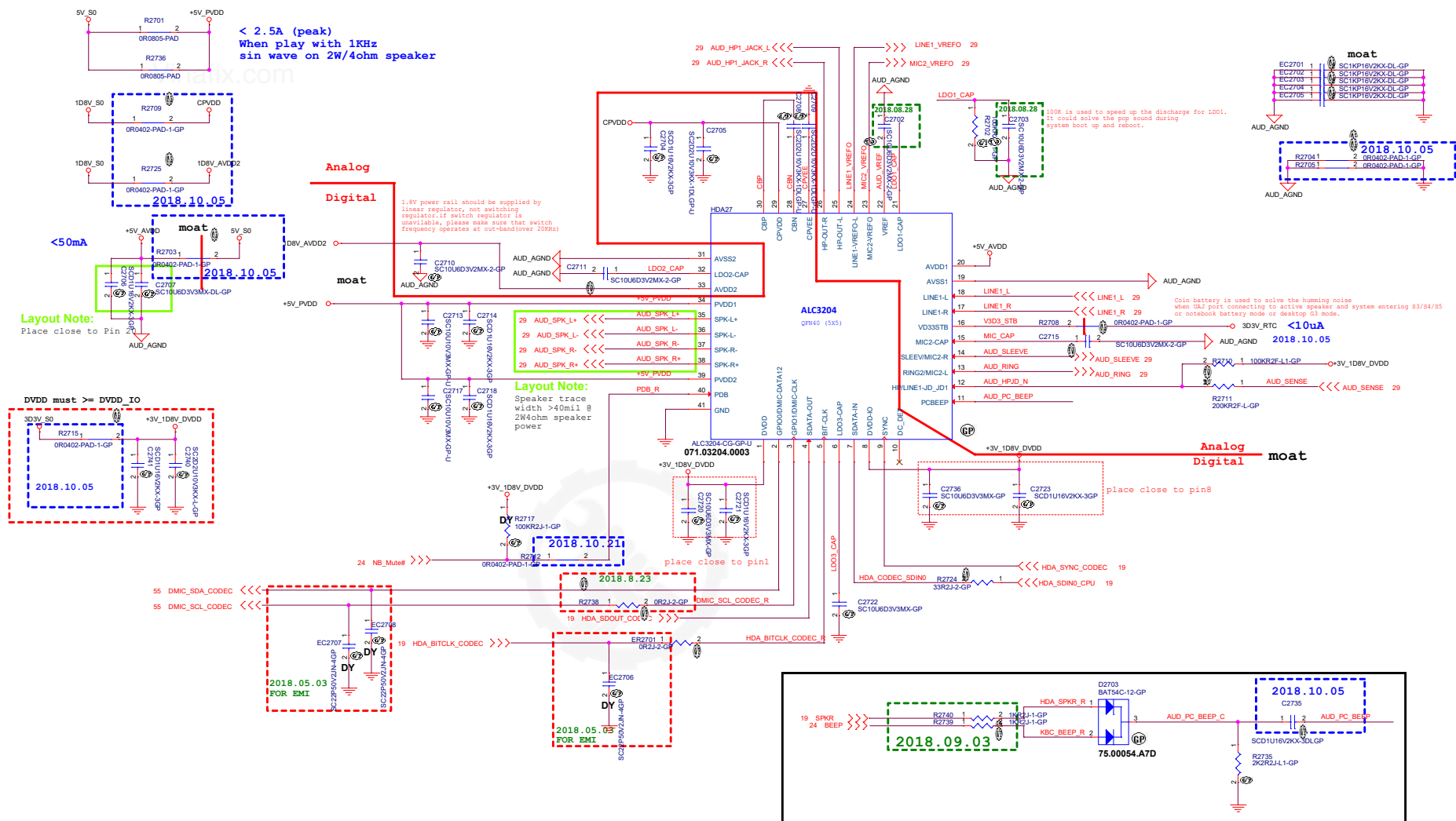
Add RTC Gen 9 reset circuit\_20170726

BOLT 15 32M 0822






**Main Func = Audio**



(Blanking)



BOLT 15 32bit 0822


		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 28 of	105



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BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 30 of	105

Main Func = LAN

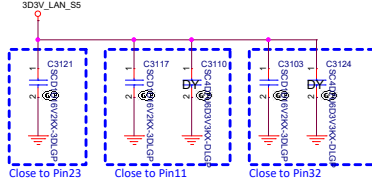
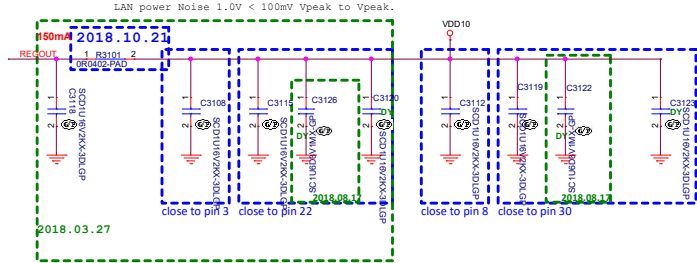
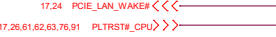
PCIE



PCIE\_CLK

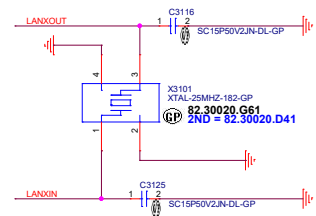
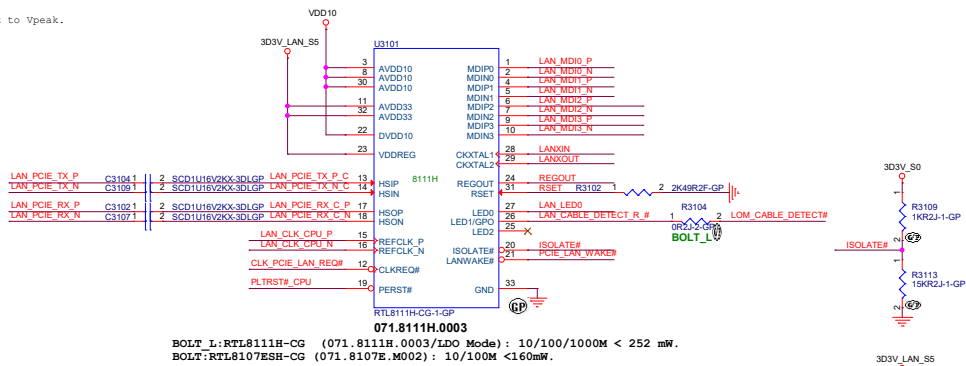


MDI



LAN CHIP (10/100/1000M & 10/100M co-lay)

3D3V\_LAN\_S5 rise time must be controlled between 0.5 ms and 100 ms.  
LAN power Noise 3.3V < 200mV Vpeak to Vpeak.



BOLT 15 32bit 0822

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **LAN RTL8106**

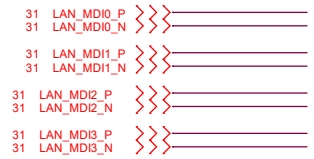
Size Document Number **BOLT WHL** Rev **A00**

Date: Thursday, December 27, 2018 Sheet 31 of 105

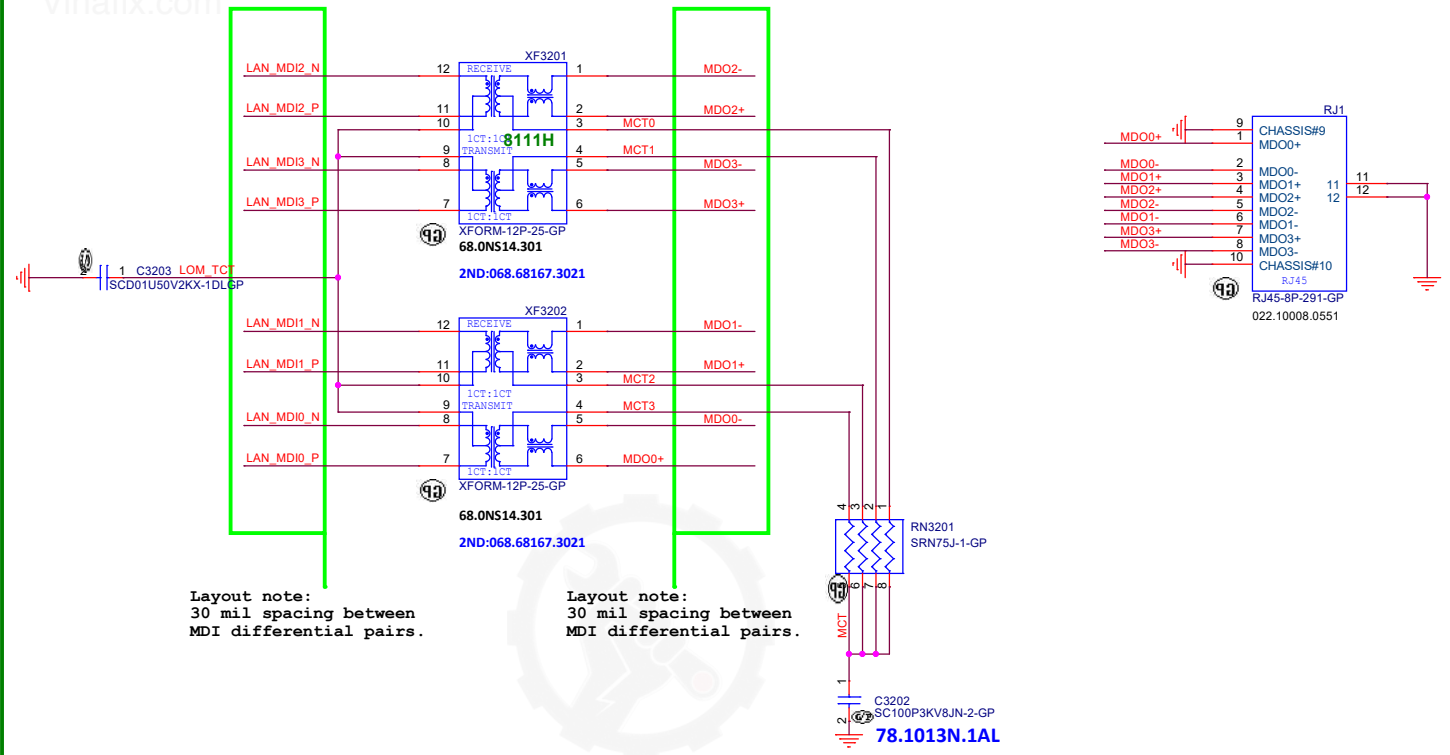
Main Func = LAN

LAN TransFormer (10/100/1000M & 10/100M co-lay)

MDI

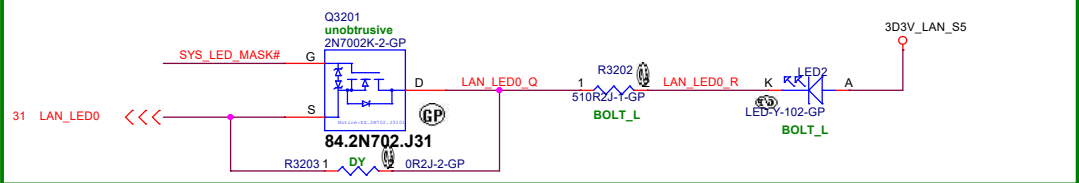


24,64 SYS\_LED\_MASK# >>>

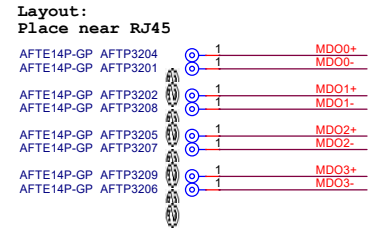


LED

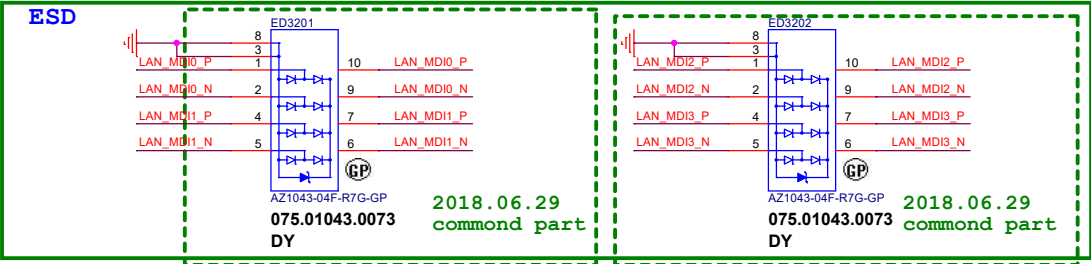
Green LED Status:  
Blinking:Data transmit (10/100/1000)  
Always Turn On: Network Connection exist  
Turn Off: No network connection exist



TEST PAD



ESD





Vinafix.com

(Blanking)



BOLT 15 32bit 0822

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Card Reader Re-driver</b>			
Size	Document Number	Rev	
A2	<b>BOLT WHL</b>		<b>A00</b>
Date: Thursday, December 27, 2018			
Sheet		32	of 105

Vinafix.com

(Blanking)



BOLT 15 32bit 0822

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB2.0 CONN</b>			
Size	Document Number		Rev
	<b>BOLT WHL</b>		<b>A00</b>
Date:	Thursday, December 27, 2018		Sheet 34 of 105

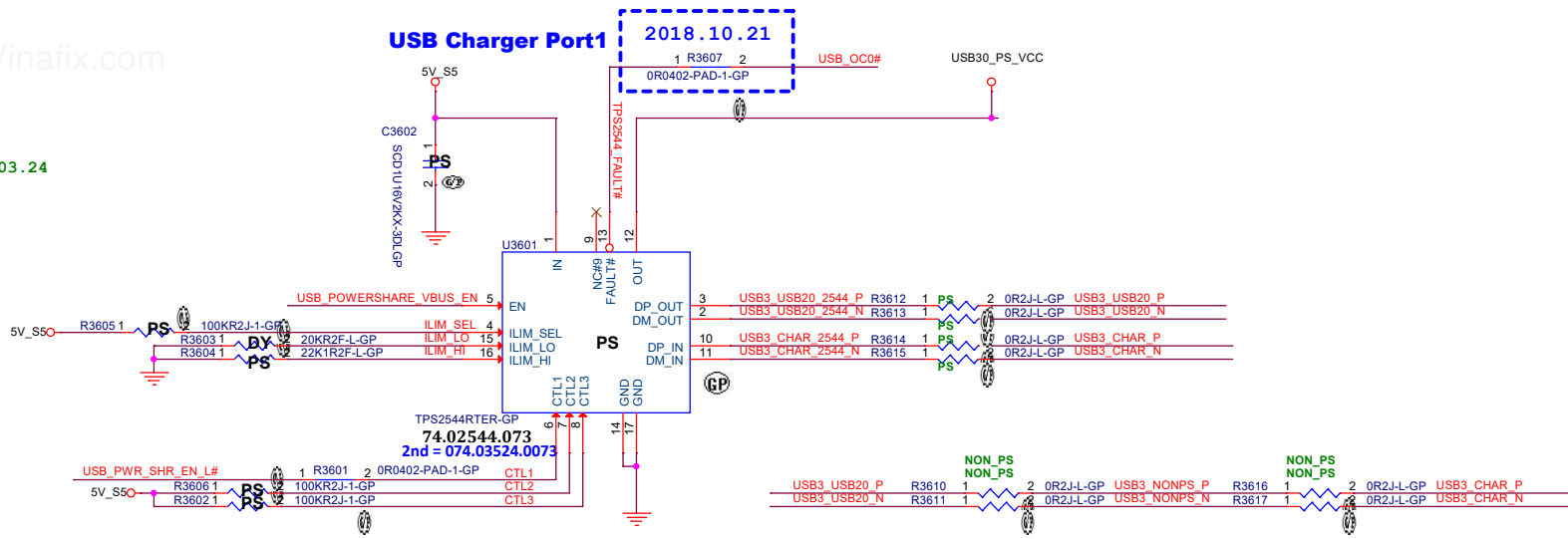


Main Func = USB Charger

2018.03.24

USB Charger Port1

2018.10.21



- 35 USB3\_CHAR\_P <<<=====
- 35 USB3\_CHAR\_N <<<=====
- 16 USB3\_USB20\_P <<<=====
- 16 USB3\_USB20\_N <<<=====
- 24 USB\_POWERSHARE\_VBUS\_EN >>>=====
- 24 USB\_PWR\_SHR\_EN\_L# >>>=====
- 16,35 USB\_OC0# <<<=====


Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS\_vp} (mA) = \frac{50,500}{(R_{ILIM\_XX} (k\Omega) + 0.1)}$$

R<sub>ILIM,XX</sub> corresponds to either R<sub>ILIM,HI</sub> or R<sub>ILIM,LO</sub> as appropriate.

BOLT 15 32bit 0822



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**USB Charger**

Size

Custom

Document Number

**BOLT WHL**

Rev

**A00**

Date:

Thursday, December 27, 2018

Sheet


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of

105

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BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB3.0 PORT</b>			
Size	Document Number		Rev
A4	<b>BOLT WHL</b>		<b>A00</b>
Date:	Thursday, December 27, 2018		Sheet 37 of 105

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Vinafix.com

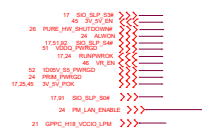
(Blanking)



BOLT 15 32bit 0822

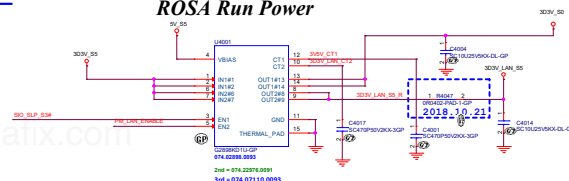
<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(RSVD)			
Size	Document Number		Rev
A2	BOLT WHL		A00
Date: Thursday, December 27, 2018			
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3D3V S0/5V S0

### ***ROSA Run Power***



## 3D3V\_S0/LAN POWER

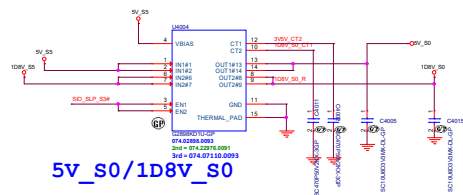
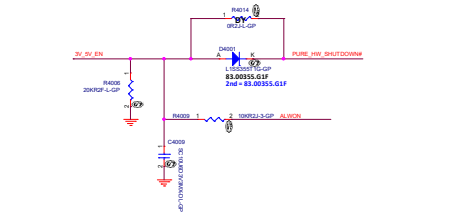


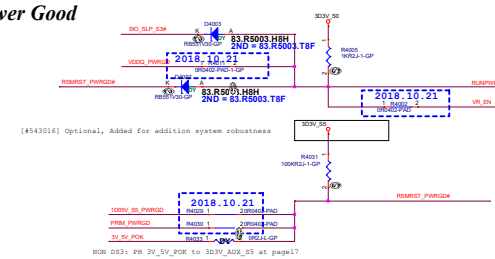
Table 4. Rise Time Values

CT (pF)	RISE TIME (pS) - 90% - 90%, C <sub>L</sub> = 0.1 pF, C <sub>00</sub> = 1.2 pF, R <sub>L</sub> = 10 Ω <sup>(1)</sup>						
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.0 V	0.6 V
0	149	112	77	70	60	56	42
220	548	388	236	206	173	154	103
470	968	673	401	342	289	256	169
1000	1768	1220	711	608	505	445	286
2200	3916	2678	1532	1067	837	749	427
4700	8040	5477	3179	2691	2240	1964	1249
10000	16520	11150	6410	5401	4430	3933	2526

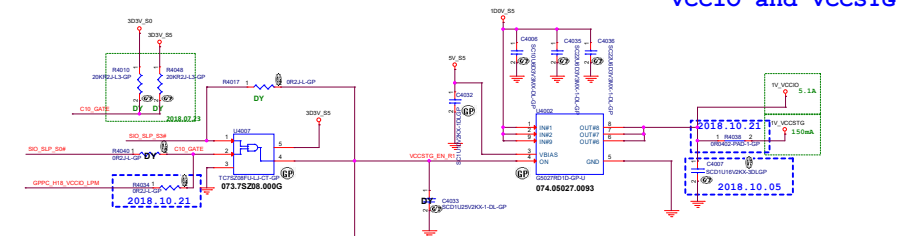
(1) TYPICAL VALUES at 25°C,  $V_{BIAS} = 5\text{ V}$ , 25 V X7R 10% CERAMIC CAP

---

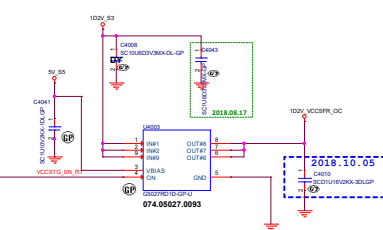
*Power Good*



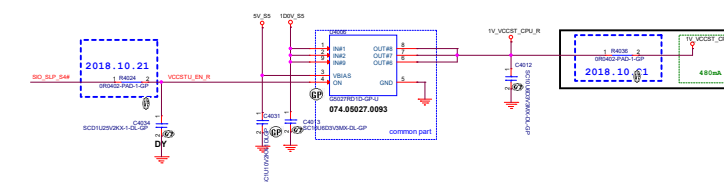
VCCIO and VCCSTG



## VCCSPLL\_OC




## VCCST/VCCPLL




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BOLT 15 32bit 0822

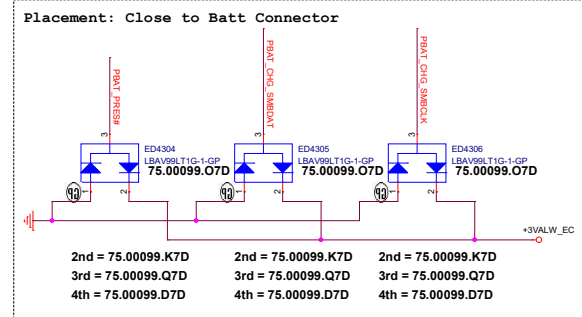
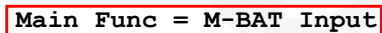
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Sequence (Modern Standby)</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 41 of	105

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BOLT 15 32bit 0822

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Connected_Standby(2/2)</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 42 of	105

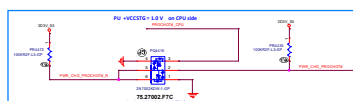
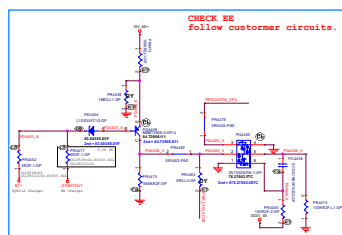
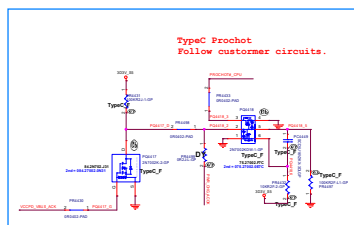
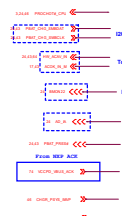
Main Func = Barrel Adapter Piug-in Detect



## ISL95522 Hybrid Charger

## Default ISL9538 Buck-Boost Charger

OFF PAGE



## BOM Change List

Year	Month	Day	Time	Location	Activity	Remarks
1990	Jan	1	10:00	Room 101	Classroom	First day of class
1990	Jan	2	10:00	Room 101	Classroom	Second day of class
1990	Jan	3	10:00	Room 101	Classroom	Third day of class
1990	Jan	4	10:00	Room 101	Classroom	Fourth day of class
1990	Jan	5	10:00	Room 101	Classroom	Fifth day of class
1990	Jan	6	10:00	Room 101	Classroom	Sixth day of class
1990	Jan	7	10:00	Room 101	Classroom	Seventh day of class
1990	Jan	8	10:00	Room 101	Classroom	Eighth day of class
1990	Jan	9	10:00	Room 101	Classroom	Ninth day of class
1990	Jan	10	10:00	Room 101	Classroom	Tenth day of class
1990	Jan	11	10:00	Room 101	Classroom	Eleventh day of class
1990	Jan	12	10:00	Room 101	Classroom	Twelfth day of class
1990	Jan	13	10:00	Room 101	Classroom	Thirteenth day of class
1990	Jan	14	10:00	Room 101	Classroom	Fourteenth day of class
1990	Jan	15	10:00	Room 101	Classroom	Fifteenth day of class
1990	Jan	16	10:00	Room 101	Classroom	Sixteenth day of class
1990	Jan	17	10:00	Room 101	Classroom	Seventeenth day of class
1990	Jan	18	10:00	Room 101	Classroom	Eighteenth day of class
1990	Jan	19	10:00	Room 101	Classroom	Nineteenth day of class
1990	Jan	20	10:00	Room 101	Classroom	Twentieth day of class
1990	Jan	21	10:00	Room 101	Classroom	Twenty-first day of class
1990	Jan	22	10:00	Room 101	Classroom	Twenty-second day of class
1990	Jan	23	10:00	Room 101	Classroom	Twenty-third day of class
1990	Jan	24	10:00	Room 101	Classroom	Twenty-fourth day of class
1990	Jan	25	10:00	Room 101	Classroom	Twenty-fifth day of class
1990	Jan	26	10:00	Room 101	Classroom	Twenty-sixth day of class
1990	Jan	27	10:00	Room 101	Classroom	Twenty-seventh day of class
1990	Jan	28	10:00	Room 101	Classroom	Twenty-eighth day of class
1990	Jan	29	10:00	Room 101	Classroom	Twenty-ninth day of class
1990	Jan	30	10:00	Room 101	Classroom	Thirtieth day of class
1990	Jan	31	10:00	Room 101	Classroom	Thirty-first day of class
1990	Feb	1	10:00	Room 101	Classroom	Thirty-second day of class
1990	Feb	2	10:00	Room 101	Classroom	Thirty-third day of class
1990	Feb	3	10:00	Room 101	Classroom	Thirty-fourth day of class
1990	Feb	4	10:00	Room 101	Classroom	Thirty-fifth day of class
1990	Feb	5	10:00	Room 101	Classroom	Thirty-sixth day of class
1990	Feb	6	10:00	Room 101	Classroom	Thirty-seventh day of class
1990	Feb	7	10:00	Room 101	Classroom	Thirty-eighth day of class
1990	Feb	8	10:00	Room 101	Classroom	Thirty-ninth day of class
1990	Feb	9	10:00	Room 101	Classroom	Fortieth day of class
1990	Feb	10	10:00	Room 101	Classroom	Forty-first day of class
1990	Feb	11	10:00	Room 101	Classroom	Forty-second day of class
1990	Feb	12	10:00	Room 101	Classroom	Forty-third day of class
1990	Feb	13	10:00	Room 101	Classroom	Forty-fourth day of class
1990	Feb	14	10:00	Room 101	Classroom	Forty-fifth day of class
1990	Feb	15	10:00	Room 101	Classroom	Forty-sixth day of class
1990	Feb	16	10:00	Room 101	Classroom	Forty-seventh day of class
1990	Feb	17	10:00	Room 101	Classroom	Forty-eighth day of class
1990	Feb	18	10:00	Room 101	Classroom	Forty-ninth day of class
1990	Feb	19	10:00	Room 101	Classroom	Fiftieth day of class
1990	Feb	20	10:00	Room 101	Classroom	Fifty-first day of class
1990	Feb	21	10:00	Room 101	Classroom	Fifty-second day of class
1990	Feb	22	10:00	Room 101	Classroom	Fifty-third day of class
1990	Feb	23	10:00	Room 101	Classroom	Fifty-fourth day of class
1990	Feb	24	10:00	Room 101	Classroom	Fifty-fifth day of class
1990	Feb	25	10:00	Room 101	Classroom	Fifty-sixth day of class
1990	Feb	26	10:00	Room 101	Classroom	Fifty-seventh day of class
1990	Feb	27	10:00	Room 101	Classroom	Fifty-eighth day of class
1990	Feb	28	10:00	Room 101	Classroom	Fifty-ninth day of class
1990	Feb	29	10:00	Room 101	Classroom	Sixtieth day of class
1990	Mar	1	10:00	Room 101	Classroom	Sixty-first day of class
1990	Mar	2	10:00	Room 101	Classroom	Sixty-second day of class
1990	Mar	3	10:00	Room 101	Classroom	Sixty-third day of class
1990	Mar	4	10:00	Room 101	Classroom	Sixty-fourth day of class
1990	Mar	5	10:00	Room 101	Classroom	Sixty-fifth day of class
1990	Mar	6	10:00	Room 101	Classroom	Sixty-sixth day of class
1990	Mar	7	10:00	Room 101	Classroom	Sixty-seventh day of class
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1990	Mar	9	10:00	Room 101	Classroom	Sixty-ninth day of class
1990	Mar	10	10:00	Room 101	Classroom	Seventieth day of class
1990	Mar	11	10:00	Room 101	Classroom	Seventy-first day of class
1990	Mar	12	10:00	Room 101	Classroom	Seventy-second day of class
1990	Mar	13	10:00	Room 101	Classroom	Seventy-third day of class
1990	Mar	14	10:00	Room 101	Classroom	Seventy-fourth day of class
1990	Mar	15	10:00	Room 101	Classroom	Seventy-fifth day of class
1990	Mar	16	10:00	Room 101	Classroom	Seventy-sixth day of class
1990	Mar	17	10:00	Room 101	Classroom	Seventy-seventh day of class
1990	Mar	18	10:00	Room 101	Classroom	Seventy-eighth day of class
1990	Mar	19	10:00	Room 101	Classroom	Seventy-ninth day of class
1990	Mar	20	10:00	Room 101	Classroom	Eightieth day of class
1990	Mar	21	10:00	Room 101	Classroom	Eighty-first day of class
1990	Mar	22	10:00	Room 101	Classroom	Eighty-second day of class
1990	Mar	23	10:00	Room 101	Classroom	Eighty-third day of class
1990	Mar	24	10:00	Room 101	Classroom	Eighty-fourth day of class
1990	Mar	25	10:00	Room 101	Classroom	Eighty-fifth day of class
1990	Mar	26	10:00	Room 101	Classroom	Eighty-sixth day of class
1990	Mar	27	10:00	Room 101	Classroom	Eighty-seventh day of class
1990	Mar	28	10:00	Room 101	Classroom	Eighty-eighth day of class
1990	Mar	29	10:00	Room 101	Classroom	Eighty-ninth day of class
1990	Mar	30	10:00	Room 101	Classroom	Ninetieth day of class
1990	Mar	31	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	1	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	2	10:00	Room 101	Classroom	Hundredth day of class
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1990	Apr	6	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	7	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	8	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	9	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	10	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	11	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	12	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	13	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	14	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	15	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	16	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	17	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	18	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	19	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	20	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	21	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	22	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	23	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	24	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	25	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	26	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	27	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	28	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	29	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	30	10:00	Room 101	Classroom	Hundredth day of class
1990	Apr	31	10:00	Room 101	Classroom	Hundredth day of class
1990	May	1	10:00	Room 101	Classroom	Hundredth day of class
1990	May	2	10:00	Room 101	Classroom	Hundredth day of class
1990	May	3	10:00	Room 101	Classroom	Hundredth day of class
1990	May	4	10:00	Room 101	Classroom	Hundredth day of class
1990	May	5	10:00	Room 101	Classroom	Hundredth day of class
1990	May	6	10:00	Room 101	Classroom	Hundredth day of class
1990	May	7	10:00	Room 101	Classroom	Hundredth day of class
1990	May	8	10:00	Room 101	Classroom	Hundredth day of class
1990	May	9	10:00	Room 101	Classroom	Hundredth day of class
1990	May	10	10:00	Room 101	Classroom	Hundredth day of class
1990	May	11	10:00	Room 101	Classroom	Hundredth day of class
1990	May	12	10:00	Room 101	Classroom	Hundredth day of class
1990	May	13	10:00	Room 101	Classroom	Hundredth day of class
1990	May	14	10:00	Room 101	Classroom	Hundredth day of class
1990	May	15	10:00	Room 101	Classroom	Hundredth day of class
1990	May	16	10:00	Room 101	Classroom	Hundredth day of class
1990	May	17	10:00	Room 101	Classroom	Hundredth day of class
1990	May	18	10:00	Room 101	Classroom	Hundredth day of class
1990	May	19	10:00	Room 101	Classroom	Hundredth day of class
1990	May	20	10:00	Room 101	Classroom	Hundredth day of class
1990	May	21	10:00	Room 101	Classroom	Hundredth day of class
1990	May	22	10:00	Room 101	Classroom	Hundredth day of class
1990	May	23	10:00	Room 101	Classroom	Hundredth day of class
1990	May	24	10:00	Room 101	Classroom	Hundredth day of class
1990	May	25	10:00	Room 101	Classroom	Hundredth day of class
1990	May	26	10:00	Room 101	Classroom	Hundredth day of class
1990	May	27	10:00	Room 101	Classroom	Hundredth day of class
1990	May	28	10:00	Room 101	Classroom	Hundredth day of class
1990	May	29	10:00	Room 101	Classroom	Hundredth day of class
1990	May	30	10:00	Room 101	Classroom	Hundredth day of class
1990	May	31	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	1	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	2	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	3	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	4	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	5	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	6	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	7	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	8	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	9	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	10	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	11	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	12	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	13	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	14	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	15	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	16	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	17	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	18	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	19	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	20	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	21	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	22	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	23	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	24	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	25	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	26	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	27	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	28	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	29	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	30	10:00	Room 101	Classroom	Hundredth day of class
1990	Jun	31	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	1	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	2	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	3	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	4	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	5	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	6	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	7	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	8	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	9	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	10	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	11	10:00	Room 101	Classroom	Hundredth day of class
1990	Jul	12				

## ISL9538

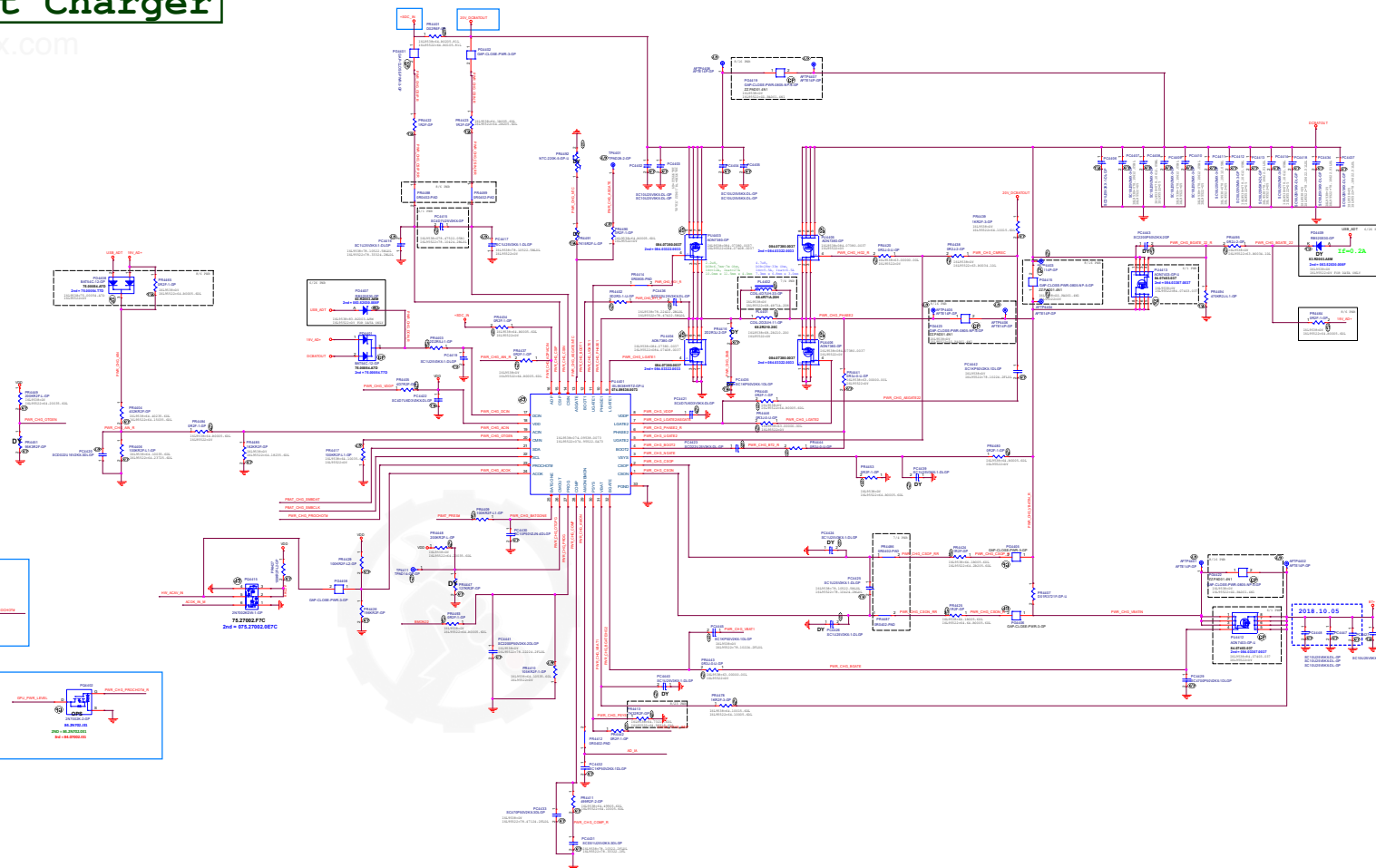
TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROGRAM RESISTANCE (s)		PROC. PER PROGRAMMING OPTIONS			
MIN	TYP MAX	CELLs	DEFAULT ROUTING FUNCTION	Automotive designing	DEFAULT ALIAS RATIO
8.45	1.45	1	7330w	No	0.475
14.5	1.45	1	7330w	No	1.5
25.0	1.50	1	1M6w	No	0.675
28.0	1.50	1	7330w	Yes	0.675
32.2	1.50	2	7330w	Yes	1.5
52.3	1.50	2	7330w	No	0.675
65.9	1.50	1	1M6w	No	0.475
75.5	1.50	1	1M6w	No	1.5
85.3	1.50	1	7330w	No	1.5
95.3	1.50	1	7330w	No	0.675
105	1.50	3	7330w	No	0.675
118	1.50	1	7330w	No	1.5
132	1.50	3	1M6w	No	0.675
147	1.50	1	1M6w	No	0.475
162	1.50	1	7330w	Yes	1.5
178	1.50	1	7330w	Yes	1.5
205	1.50	4	7330w	Yes	0.475
216	1.50	1	7330w	Yes	0.675
237	1.50	1	1M6w	No	0.675
261	1.50	1	1M6w	No	1.5
287	1.50	1	7330w	No	0.475
318	1.50	1	7330w	No	0.675

## ISL95522

Table 17. Prog Pin Programming Options

Table 11. Prog PB Performance Specimen			
Prog-GND Resistance (mΩ)	Charger Type (% Standby Resistor)	Current Sensor Resistor Value	Default # of Battery Cells in Series
22.9	0	$R_{S1} = R_{S2} = 1\Omega$	3
36.3	0	$R_{S1} = 10\Omega$ $R_{S2} = 50\Omega$	4
69.6	0	$R_{S1} = 250\Omega$ $R_{S2} = 500\Omega$	3
88.6	0	$R_{S1} = 10\Omega$ $R_{S2} = 100\Omega$	4
102	0	$R_{S1} = 10\Omega$ $R_{S2} = 250\Omega$	2
152	0	$R_{S1} = 2\Omega$ $R_{S2} = 2\Omega$	2
182	0	$R_{S1} = 2\Omega$ $R_{S2} = 2\Omega$	3
215	0	$R_{S1} = 2\Omega$ $R_{S2} = 500\Omega$	4
237	0	$R_{S1} = 50\Omega$ $R_{S2} = 50\Omega$	2
255	0	$R_{S1} = 250\Omega$ $R_{S2} = 250\Omega$	3

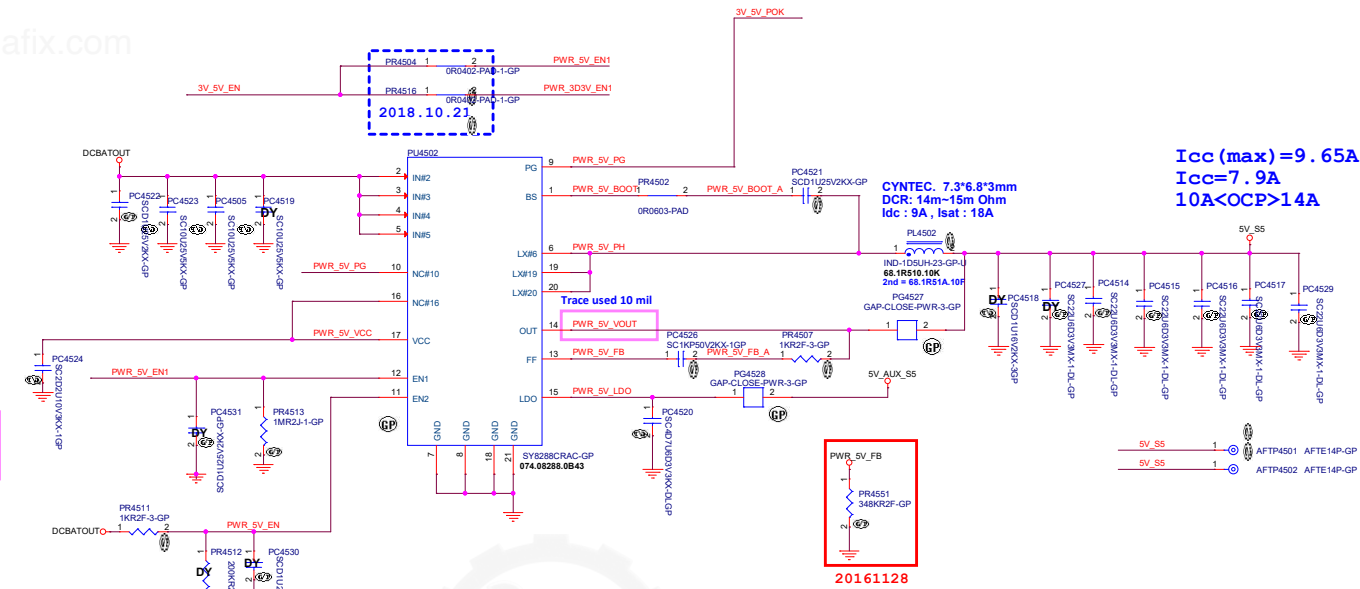


Main FUNC = PWR.Plane.Regulator\_5V

40 3V\_5V\_EN >>>  
17,25,40 3V\_5V\_POK <<<

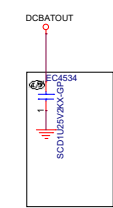
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EN rating 25V  
EN Rising Threshold : 0.8V  
Ilimit : 8A

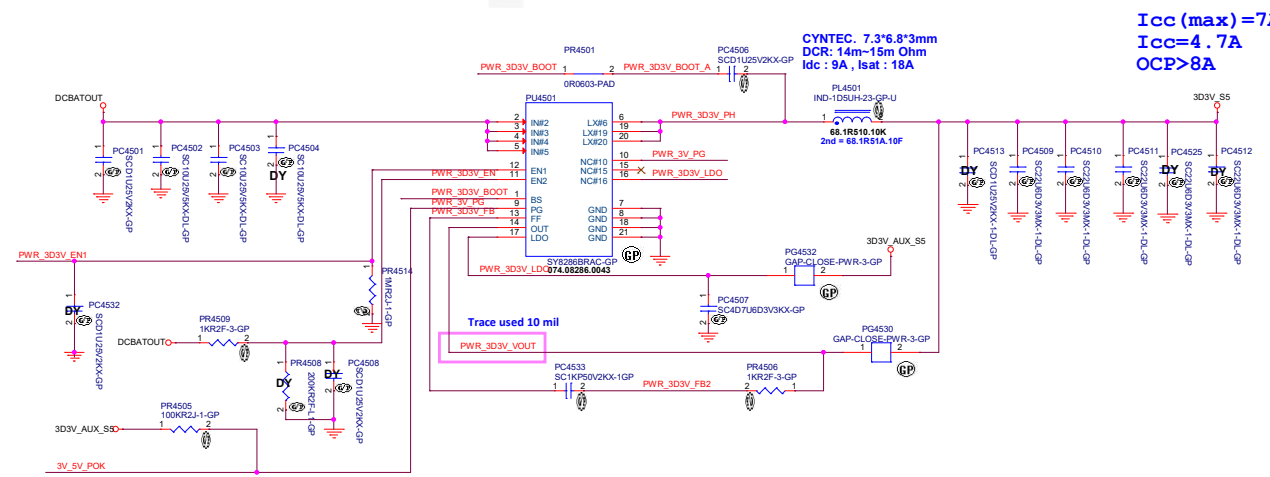


Main FUNC = PWR.Plane.Regulator\_3D3V

EN rating 25V  
EN Rising Threshold : 0.8V  
Ilimit : 8A

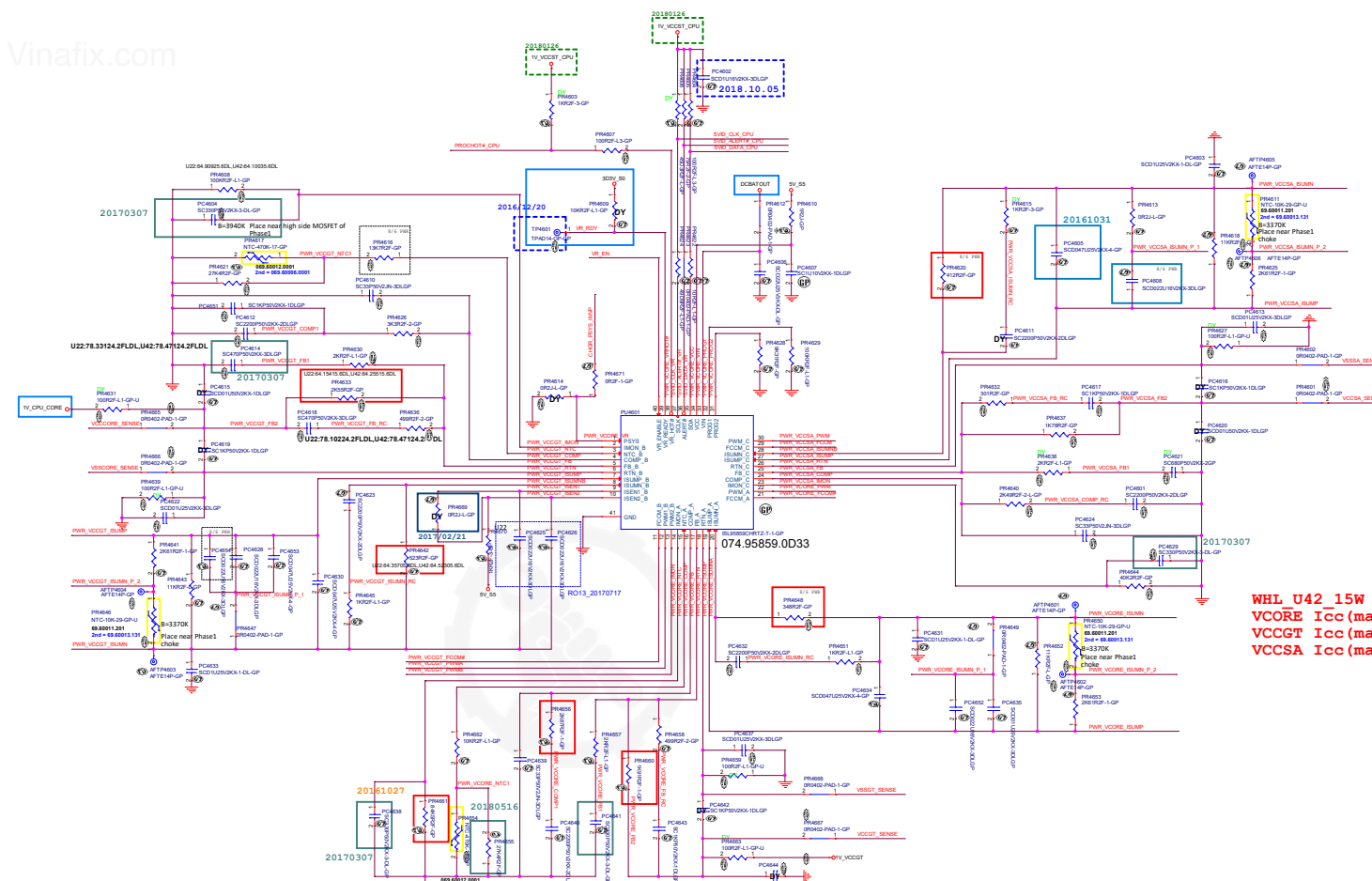


RF request 2016/01/12 modify



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48 PWR\_VCCST\_BEN1 >>>  
48 PWR\_VCCST\_BEN2 >>>

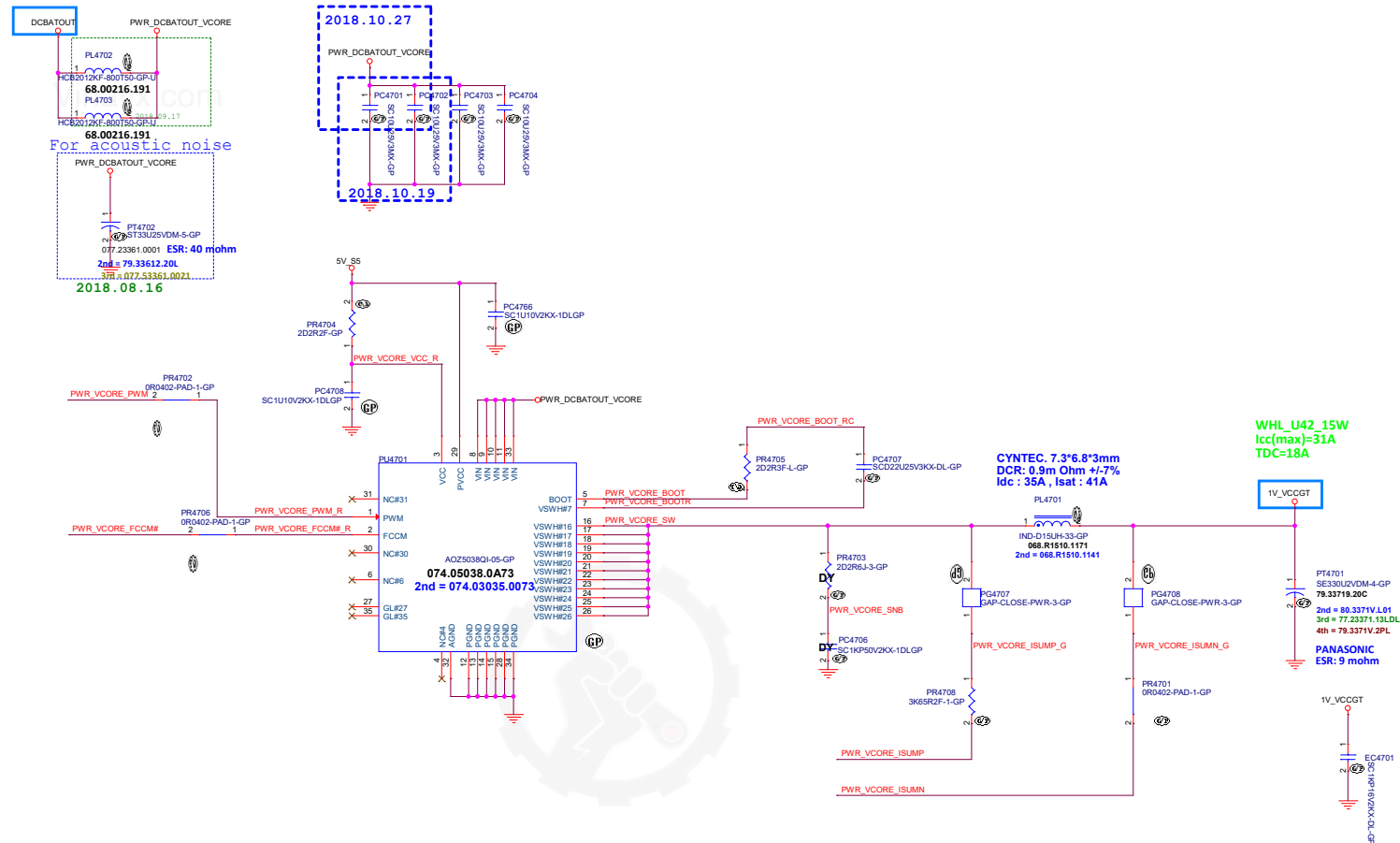
WHL\_U42\_15W  
VCORE Icc(max)=70A TDC=48 A  
VCCGT Icc(max)=31A TDC=18 A  
VCCSA Icc(max)=6A TDC=4A

	U22	U42	
PC4614	330p(78.33124.2FLDL)	470p(78.47124.2FLDL)	2017/04/25
PC4618	1Kp(78.10224.2FLDL)	470p(78.47124.2FLDL)	
PC4625	DY	0.022u(78.22321.2FLDL)	
PC4626	DY	0.022u(78.22321.2FLDL)	2017/02/21
PR4669	DY	DY	
PR4670	1K(64.10015.6DL)	DY	
PC4642	357(64.35705.6DL)	523(64.52305.6DL)	2018/04/27
PC4630	47nF(078.47322.02PD)	47nF(078.47322.02PD)	
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)	
PC4654	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)	2018/08/06
PC4653	DY	47nF(078.47322.02PD)	
PR4633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)	
PR4608	90.9K(64.90925.6DL)	100K(64.10035.6DL)	2018/04/27

# Main FUNC = CPU CORE

46 PWR\_VCORE\_PWM  
46 PWR\_VCORE\_FCCM#  
46 PWR\_VCORE\_ISUMP  
46 PWR\_VCORE\_ISUMN

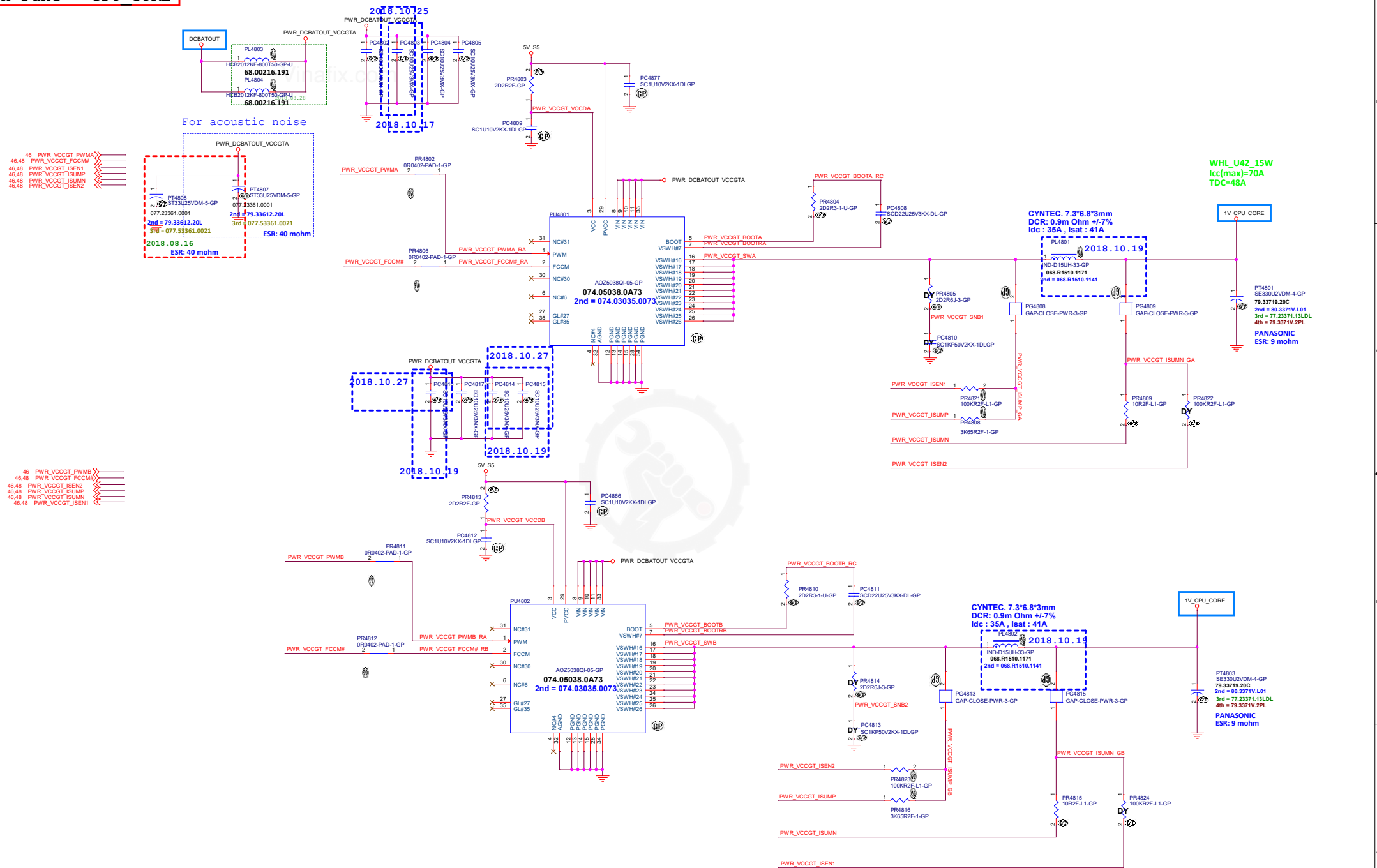
2018.09.17



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Main Func = CPU CORE



BOLT 15 32bit 0622

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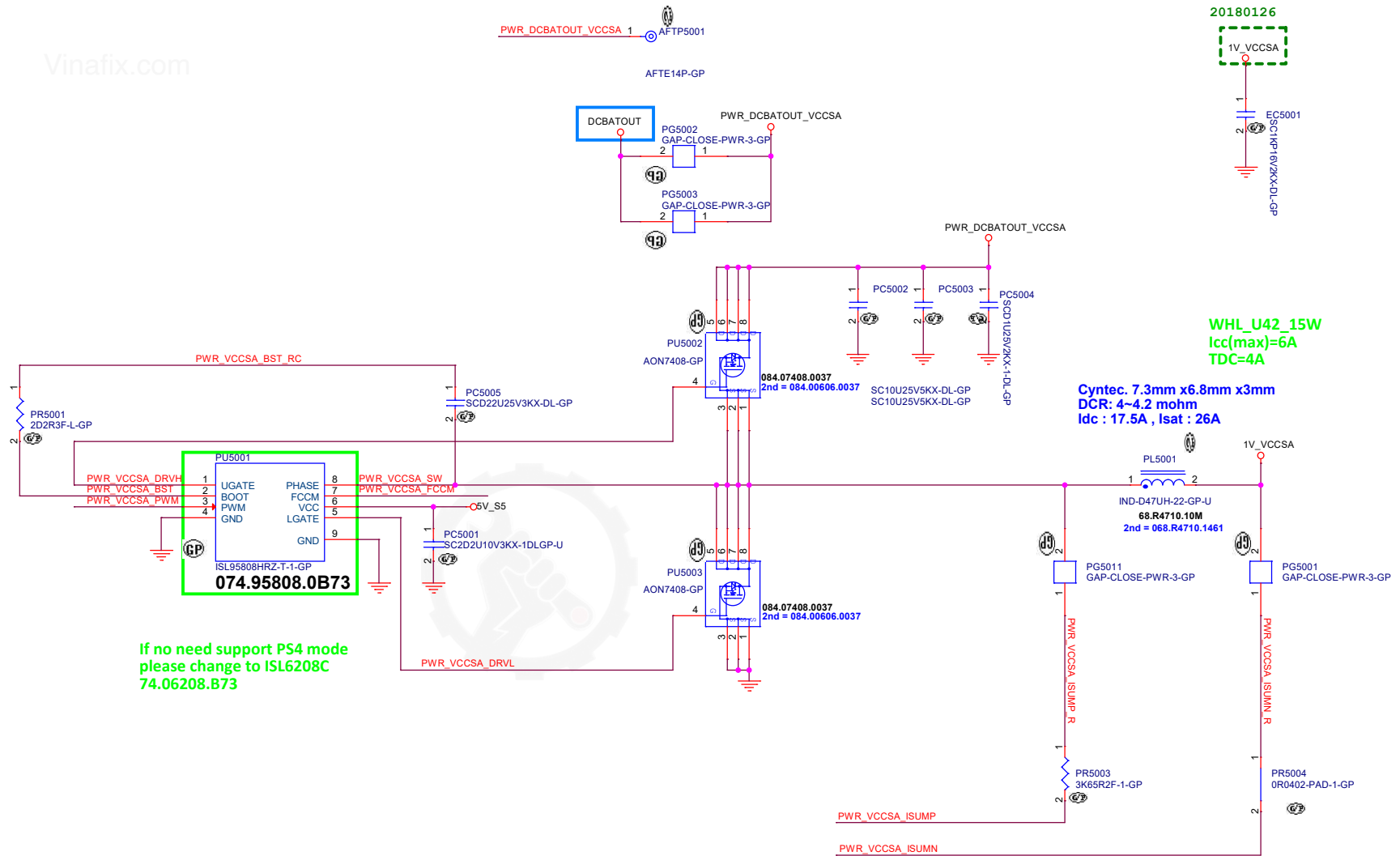
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title **NCP81210MN\_CPU\_VCCGTUS**

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**Main FUNC = CPU CORE**



If no need support PS4 mode  
please change to ISL6208C  
74.06208.B73

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	Title
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**VCCSA**

Size

Document Number	
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**BOLT WHL**

A00

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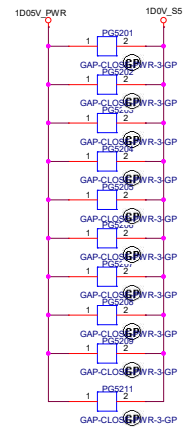
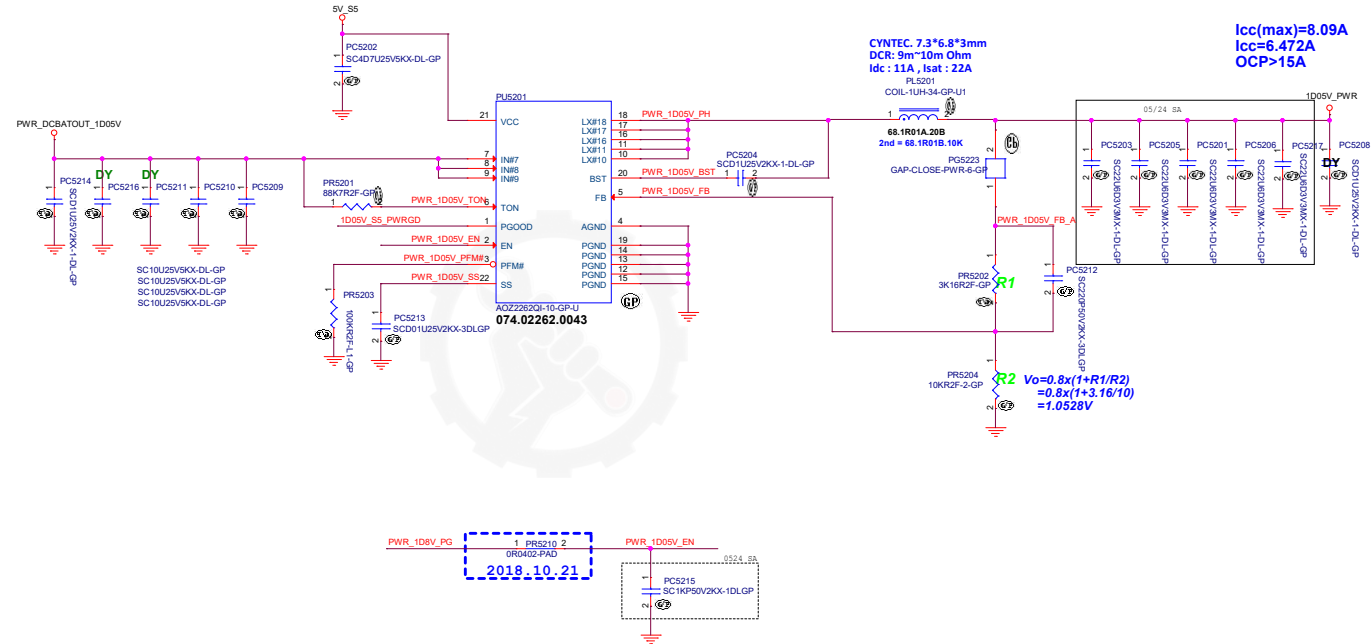
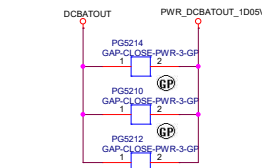
06



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# AOZ2262 for 1D05V

40 1D05V\_SS\_PWRGD <<<<  
53 PWR\_1D0V\_PG >>>>



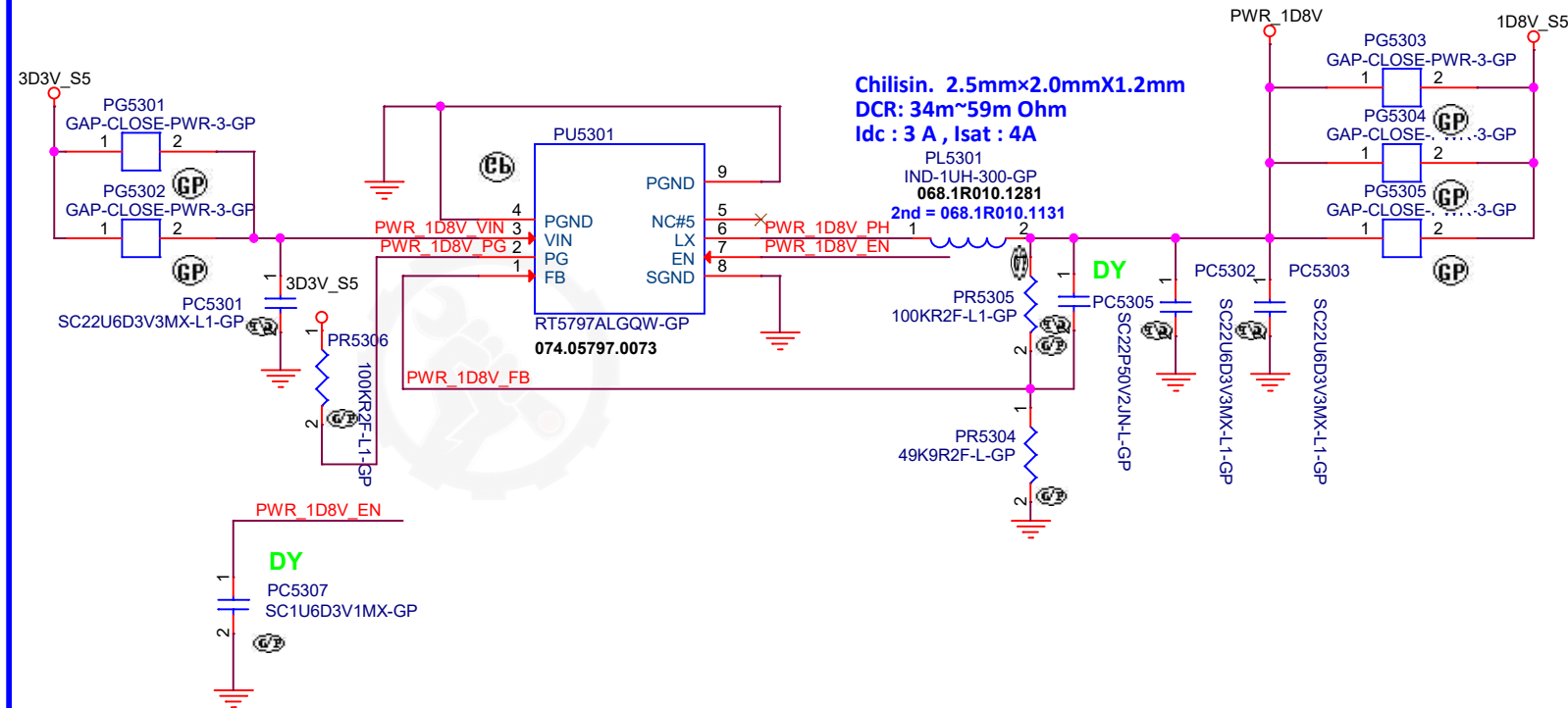
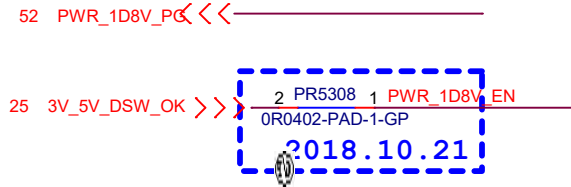
2018.10.21

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**Main Func = 1D8V**

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lcc(max)=0.902A  
lcc=0.632A  
OCP>3A



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Title
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**1D8V**

Size  
A4

Document Number
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**BOLT WHL**

Rev

# A00

Date: Thursday, December 27, 2018

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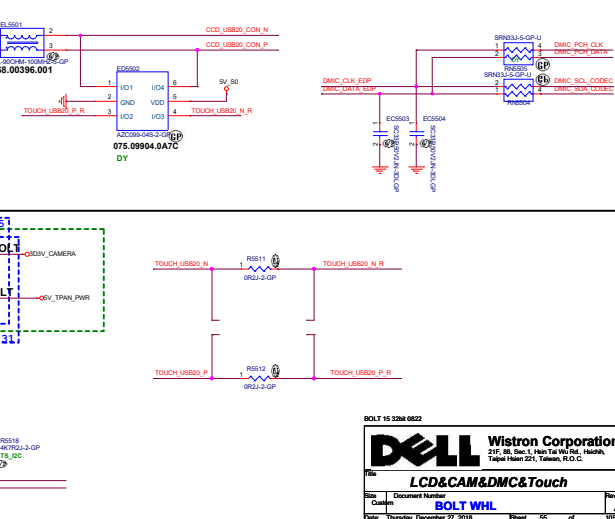
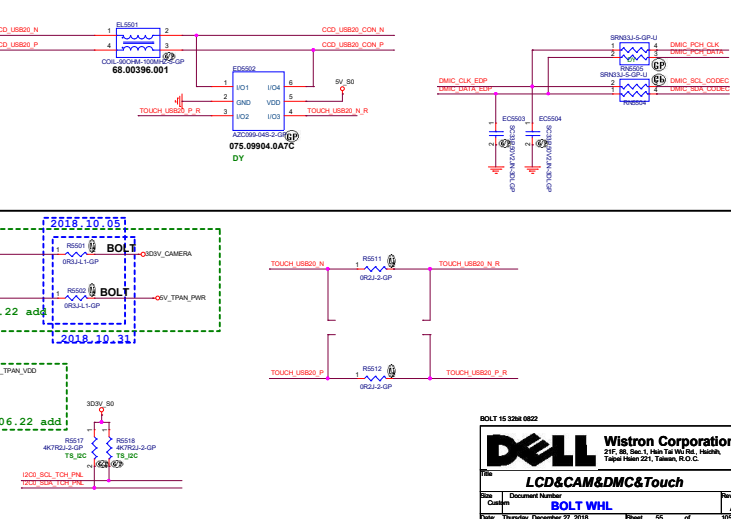
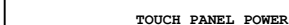
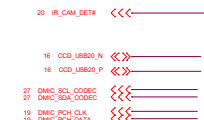
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Title			
<b>(Reserved)</b>			
Size	Document Number		Rev
Custom	<b>BOLT WHL</b>		<b>A00</b>
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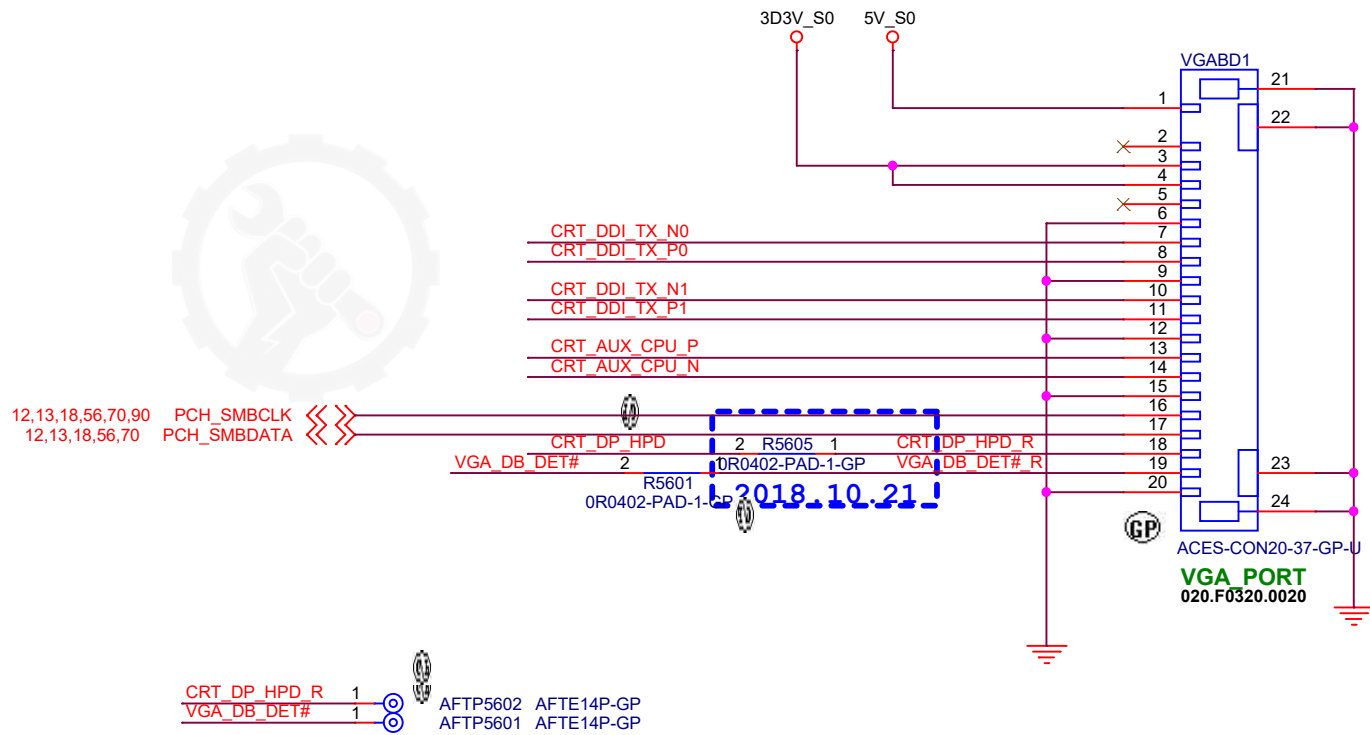
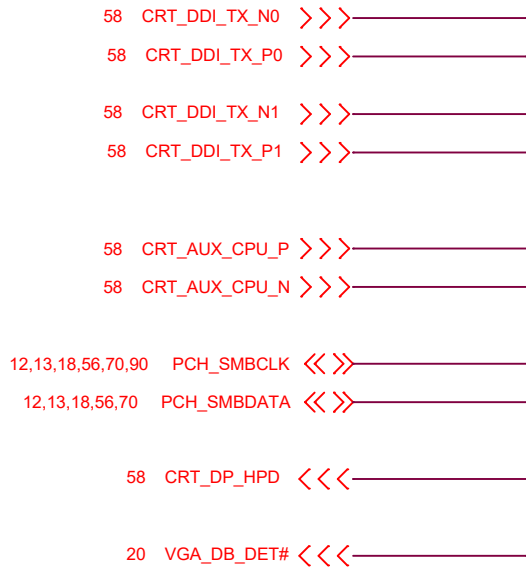
**Main Func = Touch panel**





Main Func = CRT

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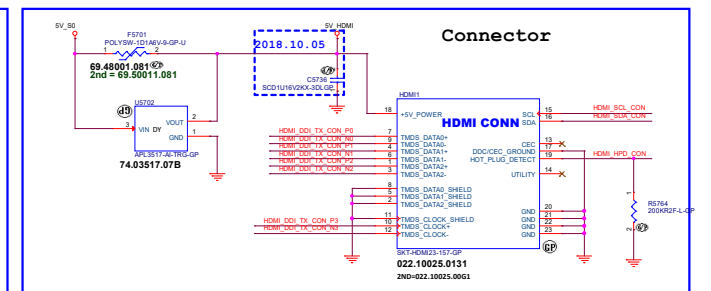
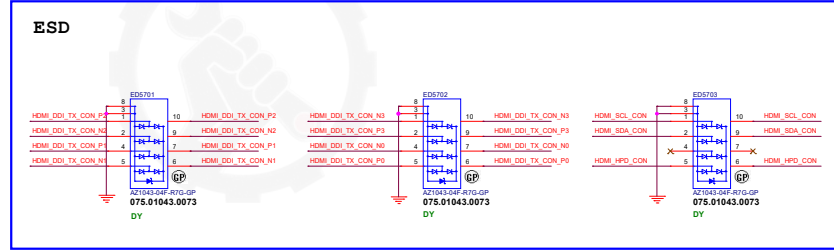
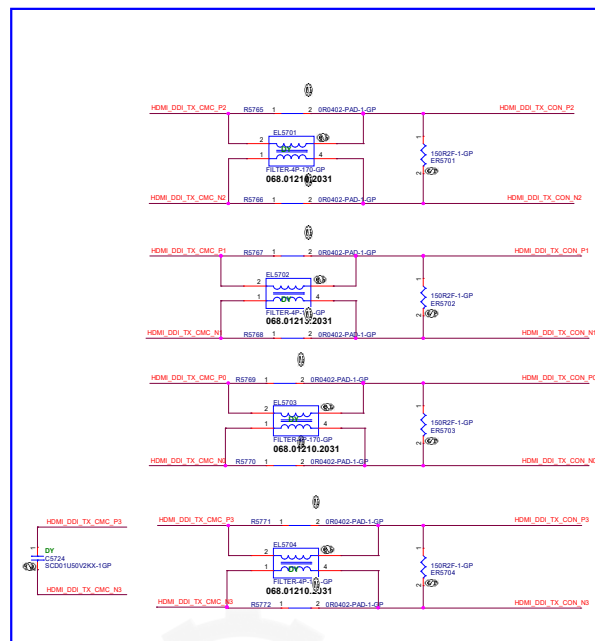
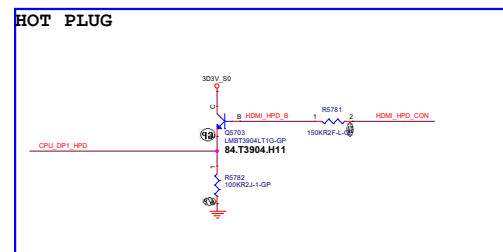
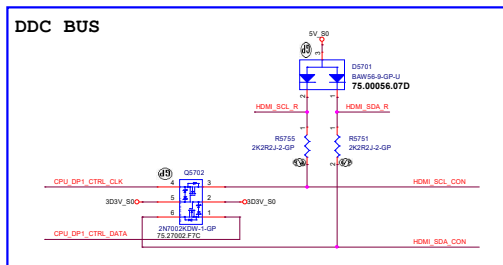
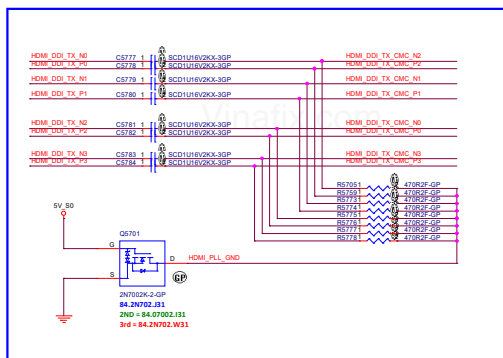
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Title <b>CRT</b>		
Size A4	Document Number <b>BOLT WHL</b>	Rev <b>A00</b>
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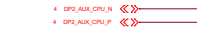
4 HDMI\_DDI\_TX\_N0 >>>  
4 HDMI\_DDI\_TX\_P0 >>>  
4 HDMI\_DDI\_TX\_N1 >>>  
4 HDMI\_DDI\_TX\_P1 >>>  
4 HDMI\_DDI\_TX\_N2 >>>  
4 HDMI\_DDI\_TX\_P2 >>>  
4 HDMI\_DDI\_TX\_N3 >>>  
4 HDMI\_DDI\_TX\_P3 >>>  
4 CPU\_DP1\_HPD <<<  
4.88 CPU\_DP1\_CTRL\_CLK <<<  
4 CPU\_DP1\_CTRL\_DATA <<<



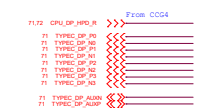
BOLT 15 32M 0822

Main Func = DP Demux

CPU DP to DP De-MUX



FOR Type C



FOR VGA



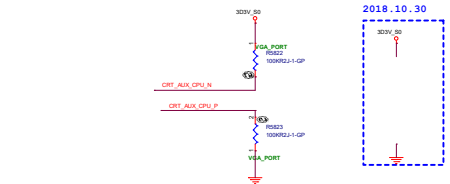
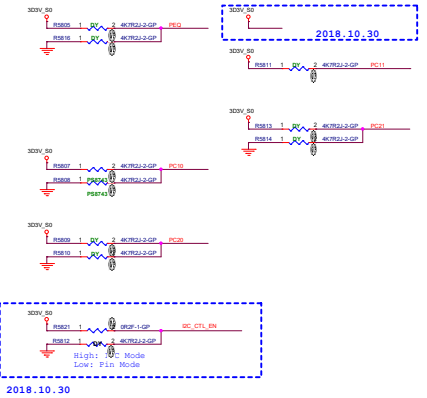
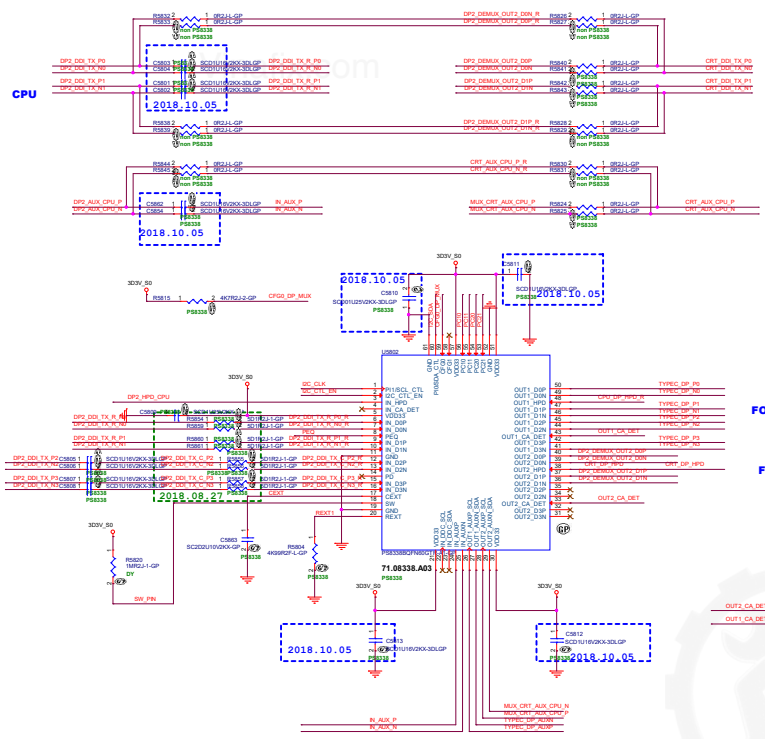
CPU

CONN

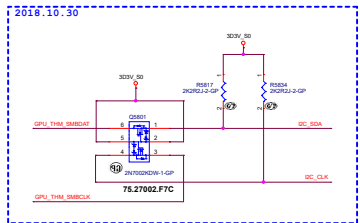
FOR Type C

FOR VGA

For AUX

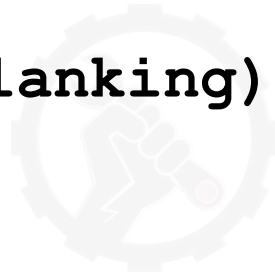


SW	I/O	Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
		For Control Switching Mode (CFG0 = L):
		SW = L: Port1 is selected (default)
		SW = H: Port2 is selected
		For Automatic Switching Mode (CFG0 = H):
		SW = L: Port1 has higher priority when both ports are plugged (default)
		SW = H: Port2 has higher priority when both ports are plugged
		Overwritten by I2C register in I2C Control Mode



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Title		(Reserved)	
Size	Document Number	Rev	
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## HDD

```

16 HDD_SATA_TX_P11 >>> _____
16 HDD_SATA_TX_N11 >>> _____

16 HDD_SATA_RX_P1K <<< _____
16 HDD_SATA_RX_N1K <<< _____


70 FFS_INT2_Q >>> _____
16 HDD_DEVSLEP >>> _____


18,20 HDD_DET# <<< _____

```

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2018.08.08

2018.10.05

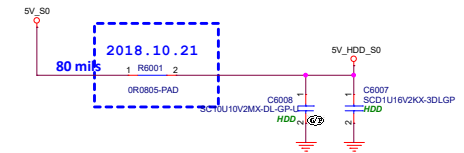
HDD_SATA_TX_P11	C6028	1	SCD01J25V2KX-3DLGP	HDD2_SATA_TX_CON_P
HDD_SATA_TX_N11	C6029	1	SCD01J25V2KX-3DLGP	HDD2_SATA_TX_CON_N
HDD_SATA_RX_N11	C6030	1	SCD01J25V2KX-3DLGP	HDD2_SATA_RX_CON_N
HDD_SATA_RX_P11	C6031	1	SCD01J25V2KX-3DLGP	HDD2_SATA_RX_CON_P

## HDD ESD

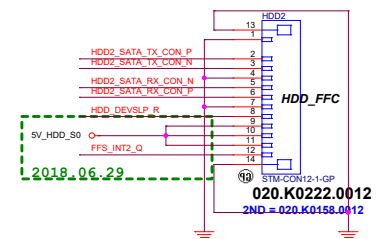
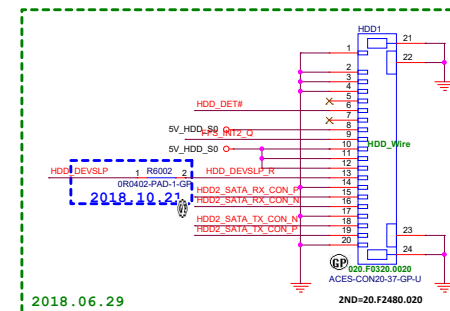
Layout Note:  
Place near HDD2

Diagram of the HD5001 component showing pin connections for HDD\_SATA\_TX\_P11, HDD\_SATA\_RX\_N11, and HDD\_SATA\_RX\_P11. The component is labeled AZ1043-04F-R7G-GP, 075.01043.0073, DY. A green box highlights the component and its pin connections, with a note "0628 change to common part" below it.

## HDD POWER



## SATA HDD Connector



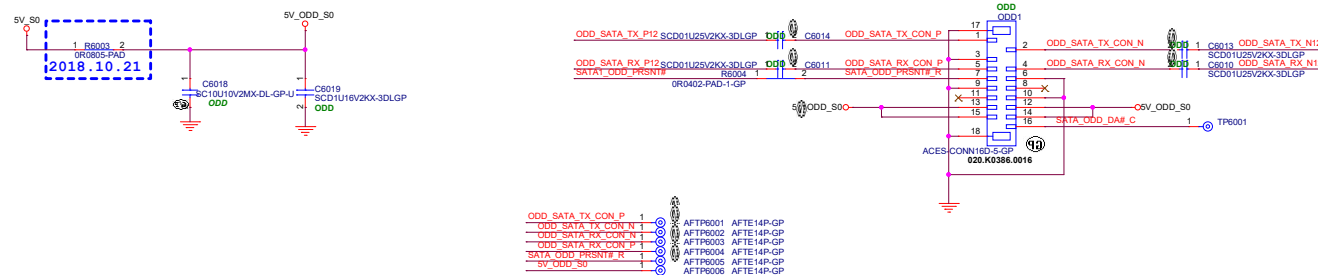
```

16  ODD_SATA_TX_N12 >>>
16  ODD_SATA_TX_P12 >>>

16  ODD_SATA_RX_P12 <<<
16  ODD_SATA_RX_N12 <<<

16  SATA1_ODD_PRSENT# >>>

```



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Title			
<b>SATA IF_HDD/ODD</b>			
Size A2	Document Number <b>BLU WHL</b>		Rev <b>A00</b>
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# Main FUNC = WLAN

## BT

21 BLUETOOTH\_EN >>>  
16 BT\_USB20\_N >>>  
16 BT\_USB20\_P >>>

## WLAN

18 CLK\_PCIE\_WLAN\_REQ# >>>  
18 WLAN\_CLK\_CPU\_N >>>  
18 WLAN\_CLK\_CPU\_P >>>  
16 WLAN\_PCIE\_RX\_N10 >>>  
16 WLAN\_PCIE\_RX\_P10 >>>  
16 WLAN\_PCIE\_TX\_N10 >>>  
16 WLAN\_PCIE\_TX\_P10 >>>

## CNVI

19 BT\_PCMFRM\_RSTN >>>  
19 BT\_PCMOUT\_CLKREQ0 >>>  
18 PULSAR\_38P4M\_REFCLK >>>  
20 CNV\_RGI\_RSP >>>  
15,20 CNV\_RGI\_DT\_R >>>  
20 CNV\_BRI\_RSP >>>  
20 CNV\_BRI\_DT\_R >>>  
21 CNV\_WT\_CLK\_DP >>>  
21 CNV\_WT\_CLK\_DN >>>  
21 CNV\_WT\_DP0 >>>  
21 CNV\_WT\_DN0 >>>  
21 CNV\_WT\_DP1 >>>  
21 CNV\_WT\_DN1 >>>  
21 CNV\_WR\_CLK\_DP >>>  
21 CNV\_WR\_CLK\_DN >>>  
21 CNV\_WR\_DP0 >>>  
21 CNV\_WR\_DN0 >>>  
21 CNV\_WR\_DP1 >>>  
21 CNV\_WR\_DN1 >>>

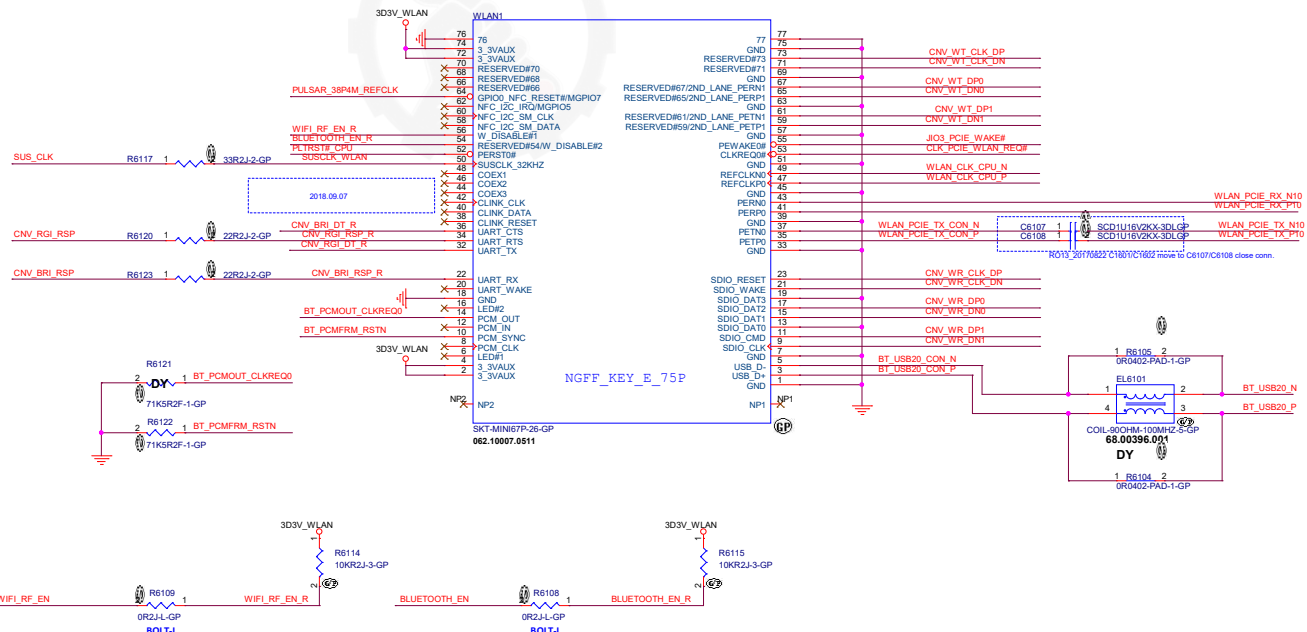
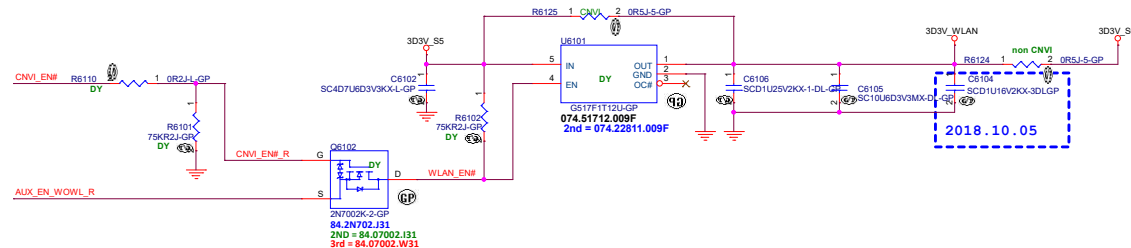
## Others

18,24 SUS\_CLK >>>  
4 CNV\_EN# >>>  
17,24 AUX\_EN\_WOVL >>>  
17,18,24 J03\_PCIE\_WAKE# <<<  
21 WIFI\_RF\_EN >>>  
17,26,31,62,63,76,91 PLTRST#\_CPU >>>

CPU		WLAN
GPP_F8_RXD	COEX1	UART TXD
GPP_F9_TXD	COEX2	UART RXD
GPP_F0_BLANKING	COEX3	STANDARD PIN

3D3V\_WLAN 1 AFTP6113  
PLTRST#\_CPU 1 AFTP6108  
BLUETOOTH\_EN 1 AFTP6112  
WIFI\_RF\_EN 1 AFTP6110  
CLK\_PCIE\_WLAN\_REQ# 1 AFTP6109  
BT\_USB20\_CON\_N 1 AFTP6111  
BT\_USB20\_CON\_P 1 AFTP6114  
J03\_PCIE\_WAKE# 1 AFTP6115

Vinafix.com

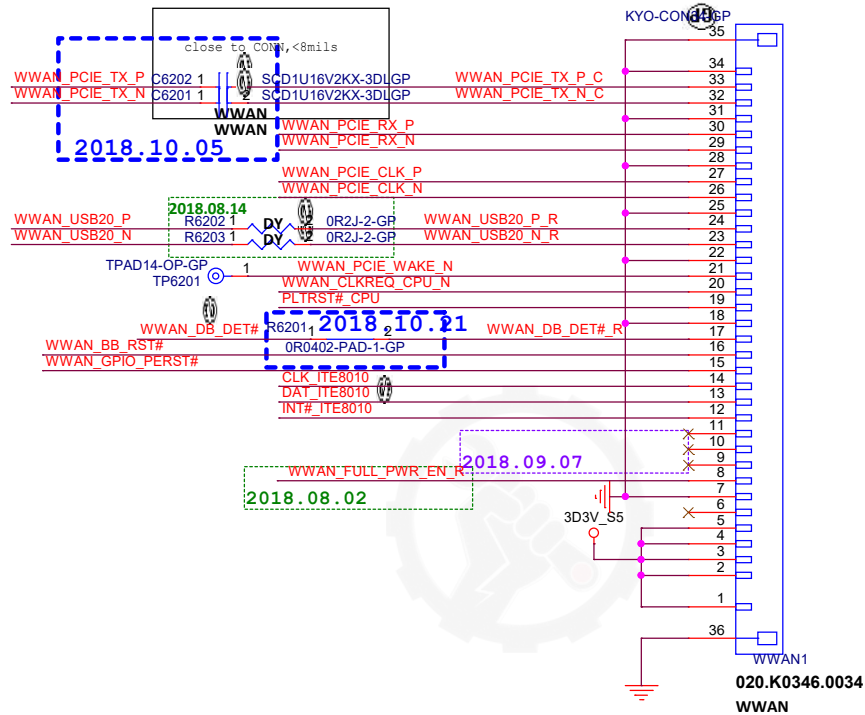
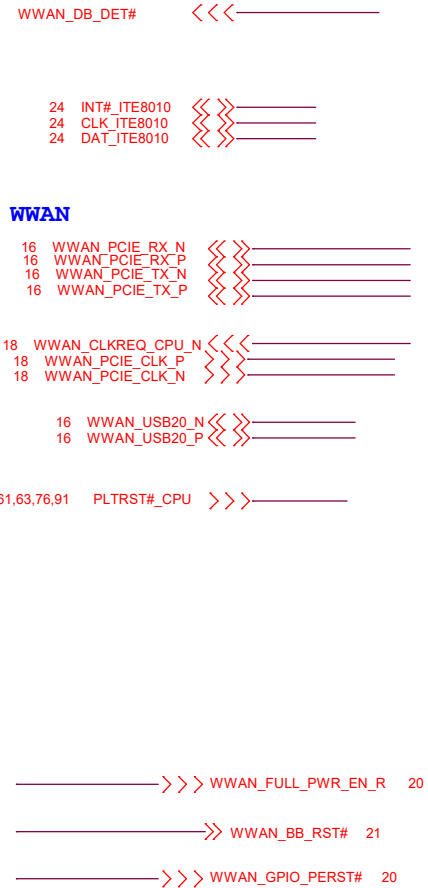


BOLT 15 32M 0622

**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title NGFF WLAN CONN  
Rev A2 Document Number BOLT WHL  
Date: Thursday, December 27, 2018 Sheet 61 of 106

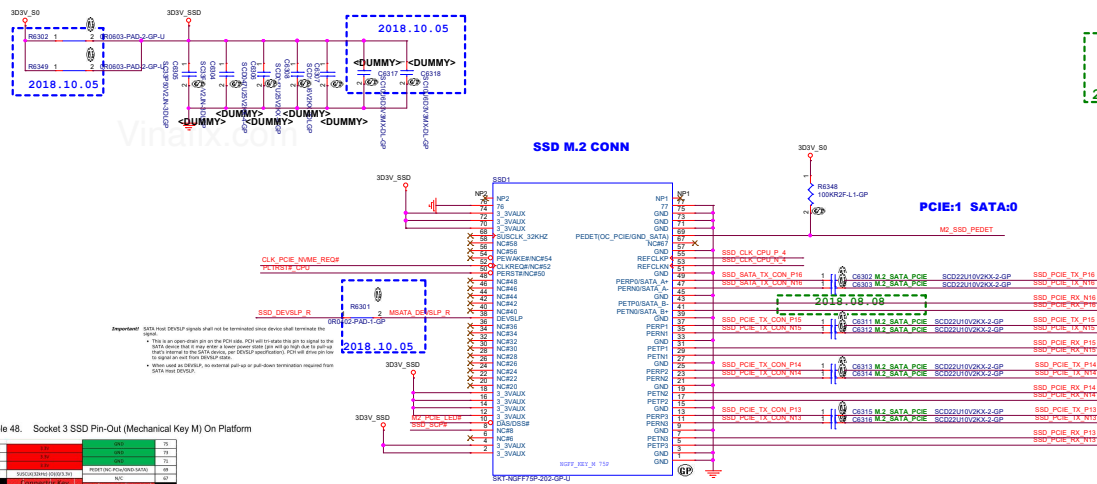
# Main FUNC = WWAN



BOLT 15 32bit 0822

<b>DELL</b>			<b>Wistron Corporation</b>		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title					
WWAN					
Size	Document Number				Rev
Custom	BOLT WHL				A00
Date:	Thursday, December 27, 2018		Sheet	62	of 105

18	SSD_PCIE_TX_F16	}}	}}
19	SSD_PCIE_TX_N16	}}	}}
20	SSD_PCIE_RX_F16	}}	}}
21	SSD_PCIE_RX_N16	}}	}}
22	SSD_PCIE_TX_F15	}}	}}
23	SSD_PCIE_TX_N15	}}	}}
24	SSD_PCIE_RX_F15	}}	}}
25	SSD_PCIE_RX_N15	}}	}}
26	SSD_PCIE_TX_F14	}}	}}
27	SSD_PCIE_TX_N14	}}	}}
28	SSD_PCIE_RX_F14	}}	}}
29	SSD_PCIE_RX_N14	}}	}}
30	SSD_PCIE_TX_F13	}}	}}
31	SSD_PCIE_TX_N13	}}	}}
32	SSD_PCIE_RX_F13	}}	}}
33	SSD_PCIE_RX_N13	}}	}}
34	SSD_PCIE_TX_F12	}}	}}
35	SSD_PCIE_TX_N12	}}	}}
36	SSD_PCIE_RX_F12	}}	}}
37	SSD_PCIE_RX_N12	}}	}}
38	SSD_PCIE_TX_F11	}}	}}
39	SSD_PCIE_TX_N11	}}	}}
40	SSD_PCIE_RX_F11	}}	}}
41	SSD_PCIE_RX_N11	}}	}}
42	SSD_PCIE_TX_F10	}}	}}
43	SSD_PCIE_TX_N10	}}	}}
44	SSD_PCIE_RX_F10	}}	}}
45	SSD_PCIE_RX_N10	}}	}}
46	SSD_PCIE_TX_F9	}}	}}
47	SSD_PCIE_TX_N9	}}	}}
48	SSD_PCIE_RX_F9	}}	}}
49	SSD_PCIE_RX_N9	}}	}}
50	SSD_PCIE_TX_F8	}}	}}
51	SSD_PCIE_TX_N8	}}	}}
52	SSD_PCIE_RX_F8	}}	}}
53	SSD_PCIE_RX_N8	}}	}}
54	SSD_PCIE_TX_F7	}}	}}
55	SSD_PCIE_TX_N7	}}	}}
56	SSD_PCIE_RX_F7	}}	}}
57	SSD_PCIE_RX_N7	}}	}}
58	SSD_PCIE_TX_F6	}}	}}
59	SSD_PCIE_TX_N6	}}	}}
60	SSD_PCIE_RX_F6	}}	}}
61	SSD_PCIE_RX_N6	}}	}}
62	SSD_PCIE_TX_F5	}}	}}
63	SSD_PCIE_TX_N5	}}	}}
64	SSD_PCIE_RX_F5	}}	}}
65	SSD_PCIE_RX_N5	}}	}}
66	SSD_PCIE_TX_F4	}}	}}
67	SSD_PCIE_TX_N4	}}	}}
68	SSD_PCIE_RX_F4	}}	}}
69	SSD_PCIE_RX_N4	}}	}}
70	SSD_PCIE_TX_F3	}}	}}
71	SSD_PCIE_TX_N3	}}	}}
72	SSD_PCIE_RX_F3	}}	}}
73	SSD_PCIE_RX_N3	}}	}}
74	SSD_PCIE_TX_F2	}}	}}
75	SSD_PCIE_TX_N2	}}	}}
76	SSD_PCIE_RX_F2	}}	}}
77	SSD_PCIE_RX_N2	}}	}}
78	SSD_PCIE_TX_F1	}}	}}
79	SSD_PCIE_TX_N1	}}	}}
80	SSD_PCIE_RX_F1	}}	}}
81	SSD_PCIE_RX_N1	}}	}}
82	SSD_PCIE_TX_F0	}}	}}
83	SSD_PCIE_TX_N0	}}	}}
84	SSD_PCIE_RX_F0	}}	}}
85	SSD_PCIE_RX_N0	}}	}}
86	SSD_PCIE_TX_F0	}}	}}
87	SSD_PCIE_TX_N0	}}	}}
88	SSD_PCIE_RX_F0	}}	}}
89	SSD_PCIE_RX_N0	}}	}}
90	SSD_PCIE_TX_F0	}}	}}
91	SSD_PCIE_TX_N0	}}	}}
92	SSD_PCIE_RX_F0	}}	}}
93	SSD_PCIE_RX_N0	}}	}}
94	SSD_PCIE_TX_F0	}}	}}
95	SSD_PCIE_TX_N0	}}	}}
96	SSD_PCIE_RX_F0	}}	}}
97	SSD_PCIE_RX_N0	}}	}}
98	SSD_PCIE_TX_F0	}}	}}
99	SSD_PCIE_TX_N0	}}	}}
100	SSD_PCIE_RX_F0	}}	}}
101	SSD_PCIE_RX_N0	}}	}}
102	SSD_PCIE_TX_F0	}}	}}
103	SSD_PCIE_TX_N0	}}	}}
104	SSD_PCIE_RX_F0	}}	}}
105	SSD_PCIE_RX_N0	}}	}}
106	SSD_PCIE_TX_F0	}}	}}
107	SSD_PCIE_TX_N0	}}	}}
108	SSD_PCIE_RX_F0	}}	}}
109	SSD_PCIE_RX_N0	}}	}}
110	SSD_PCIE_TX_F0	}}	}}
111	SSD_PCIE_TX_N0	}}	}}
112	SSD_PCIE_RX_F0	}}	}}
113	SSD_PCIE_RX_N0	}}	}}
114	SSD_PCIE_TX_F0	}}	}}
115	SSD_PCIE_TX_N0	}}	}}
116	SSD_PCIE_RX_F0	}}	}}
117	SSD_PCIE_RX_N0	}}	}}
118	SSD_PCIE_TX_F0	}}	}}
119	SSD_PCIE_TX_N0	}}	}}
120	SSD_PCIE_RX_F0	}}	}}
121	SSD_PCIE_RX_N0		

[illegible]

Condition	PCIe Gen2* Gen 2 Only	PCIe Gen3* Gen 3 Only	SATA Only	PCIe Express* Gen 2 / SATA	PCIe Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

**Notes:**

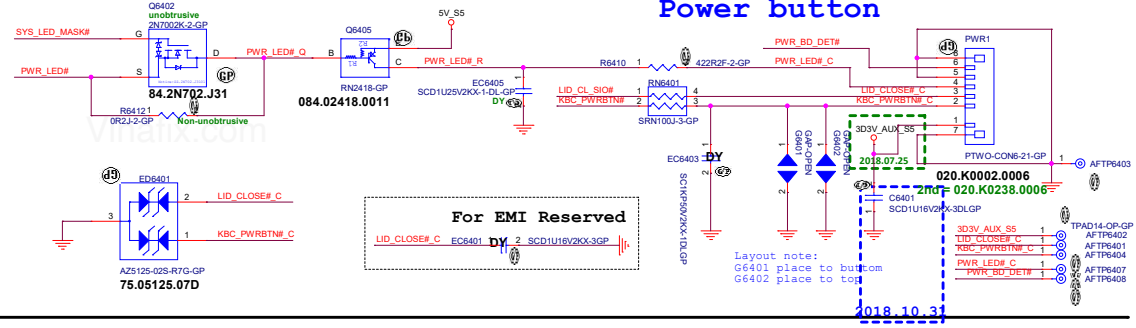
- Design Constraint: For PCIe Only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe\* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices** as a Design Constraint: For PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices** as a Design Constraint: For SATA only configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices** as a Design Constraint: For SATA only configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**



Main Func = Power BTN

24 PWR\_LED# >>> \_\_\_\_\_  
20.21 PWR\_BD\_DET# <<< \_\_\_\_\_  
24.92 LID\_CL\_SIO# <<< \_\_\_\_\_  
24.92 KBC\_PWRBTN# <<< \_\_\_\_\_

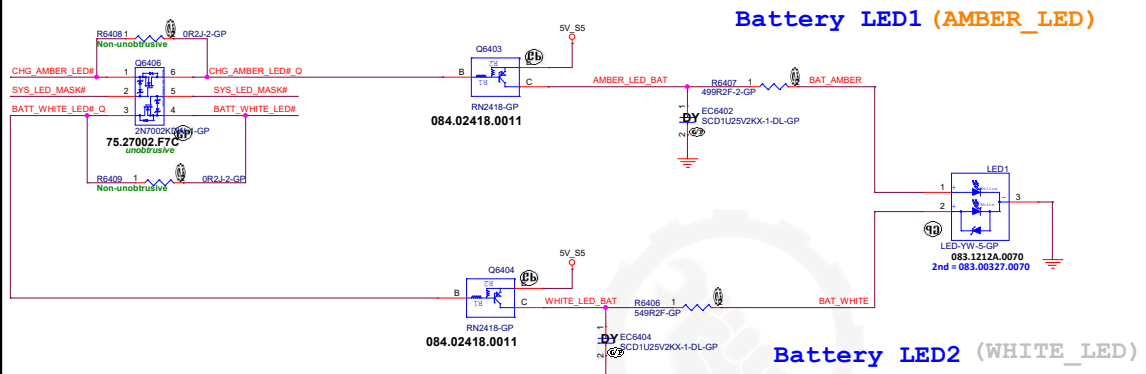
NONE FINGER PRINT 才會上件



Main Func = Battery LED

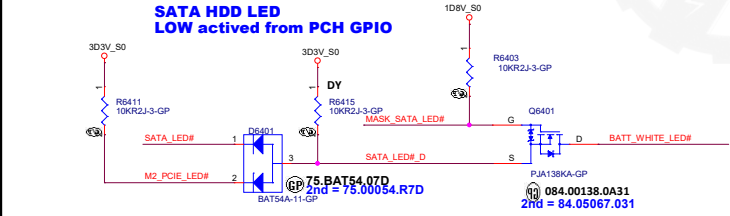
Low activated from KBC GPIO

24.32 SYS\_LED\_MASK# >>> \_\_\_\_\_  
24 CHG\_AMBER\_LED# >>> \_\_\_\_\_  
24 BATT\_WHITE\_LED# >>> \_\_\_\_\_



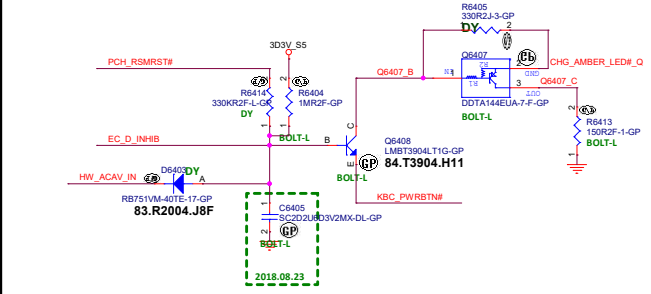
Main Func = HDD LED

24 MASK\_SATA\_LED# >>> \_\_\_\_\_  
16 SATA\_LED# >>> \_\_\_\_\_  
63 M2\_PCIE\_LED# <<< \_\_\_\_\_



Main Func = M-BIST

17.24 PCH\_RSMRST# >>> \_\_\_\_\_  
24 EC\_D\_IN#B >>> \_\_\_\_\_  
24.43.44 HW\_ACAV\_IN >>> \_\_\_\_\_



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

24 CAP\_LED#\_R >>>

24 KSQ[0..7] >>>

24 KSQ[0..16] <<<

20 KB\_DET# <<<

KB\_LED\_BL\_DET <<<

24 KB\_LED\_PWM >>>

[illegible][illegible]

ACES-CON30-29-GP  
**020.K0254.0030**  
**2nd = 020.K0274.0030**  
**3rd = 20.K0750.030**

24 TP\_EN# >>> \_\_\_\_\_

24 CLK\_TP\_SIO <<< \_\_\_\_\_

24 DAT\_TP\_SIO <<< \_\_\_\_\_

I2C0\_SCL\_TCH\_PAD >>> \_\_\_\_\_

I2C0\_SDA\_TCH\_PAD >>> \_\_\_\_\_

24 TP\_WAKE\_KBC# <<< \_\_\_\_\_

24 PTP\_DIS# >>> \_\_\_\_\_

[illegible]

TP side has pull high

TP WAKE\_KBC# 1 R6511 2 TP\_VDD

10KR2J-3-GM

TP\_WAKE

**Precision Touch Pad Connector**

TP\_VDD

C5005

SCD1WV2004-02

49P-Touch Pad Connector

TP1

ACES-CON8-66-GP

020.K0151.0008

2ND=020.K0255.0008

AFTP6531

I2C1\_SDA\_R

I2C1\_SCL\_R

TP\_WAKE\_KBCIF

PTP\_DIS#

I2C1A\_C

TPCLK\_C

AFTP6529

AFTP6528

AFTP6527

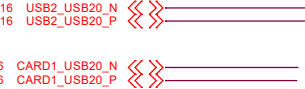
AFTP6526

Signal	Pin
TP_VDD	1
TPCLK_C	1
I2C1A_C	1
I2C1_SCL_R	1
I2C1_SDA_R	1
TP_WAKE_KBCIF	1
PTP_DIS#	1

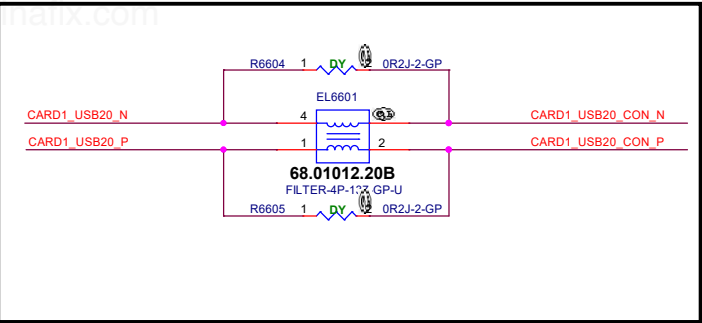
Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

Main Func = IO Connector

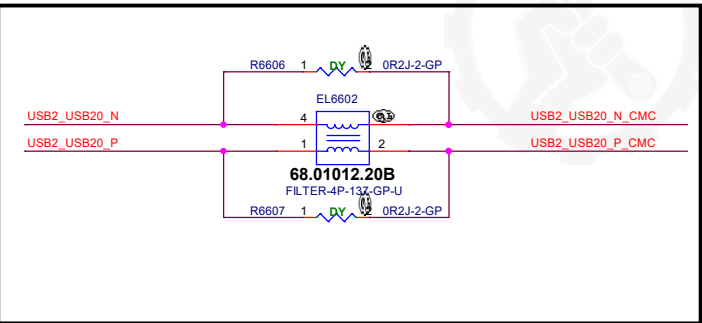
USB 2.0



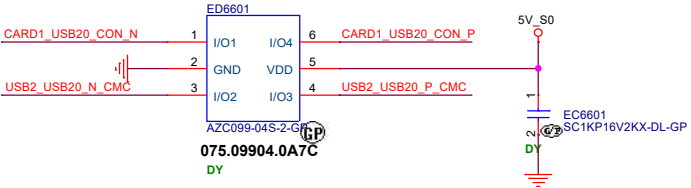
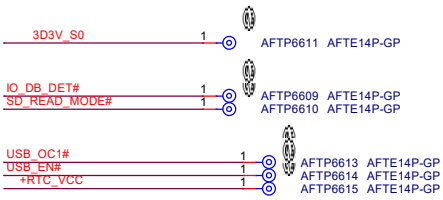
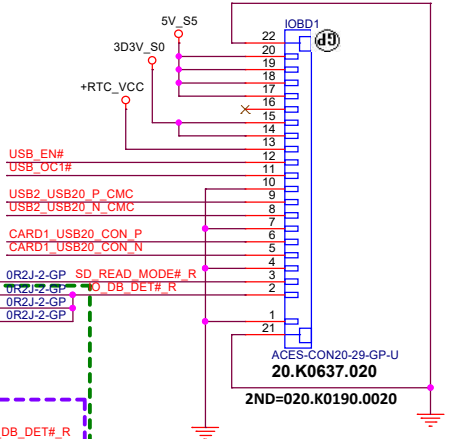
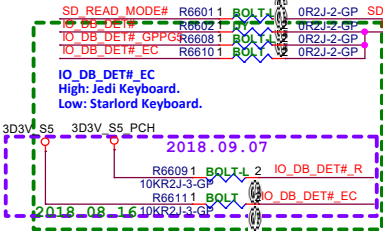
USB2.0 CARD



USB2.0 CARD



USB2.0 Card Reader SD3.0



BOLT 15 32bit 0822

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**

Size	Document Number	Rev
Custom	<b>BOLT WHL</b>	<b>A00</b>
Date:	Thursday, December 27, 2018	Sheet 66 of 105

(Blanking)

BOLT 15 32bit 0822



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Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size  
A4

Document Number

**BOLT WHL**

Rev

**A00**

Date: Thursday, December 27, 2018

Sheet 67 of 105

# Main Func = Debug

Vinafix.com

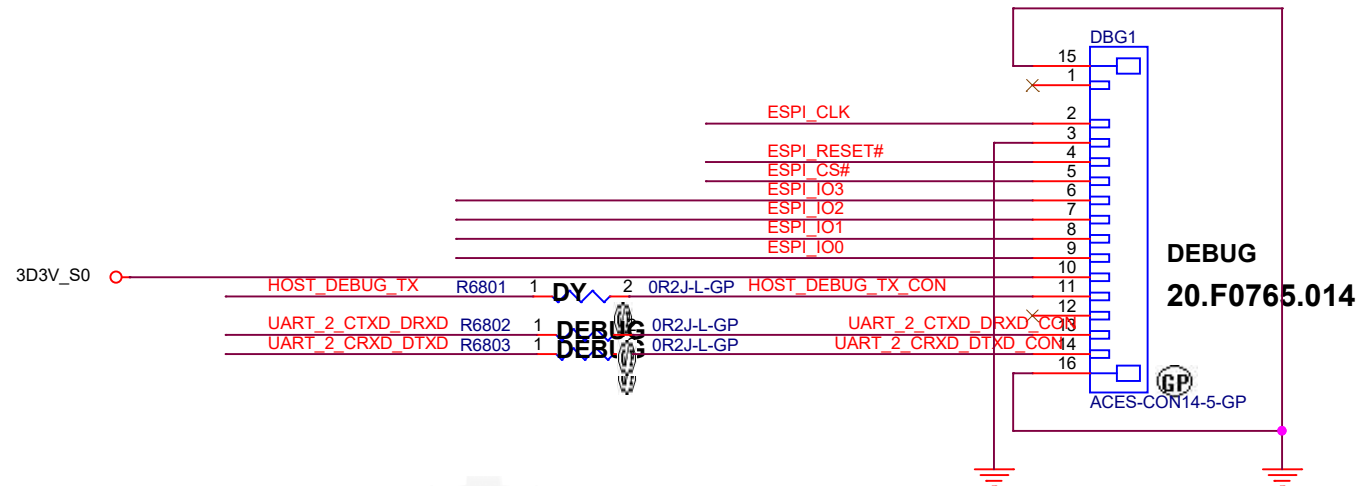
18,24 ESPI\_CLK  
18,24 ESPI\_RESET#  
18,24 ESPI\_CS#

24 HOST\_DEBUG\_TX  
20 UART\_2\_CTXD\_DRXD  
20 UART\_2\_CRXD\_DTXD

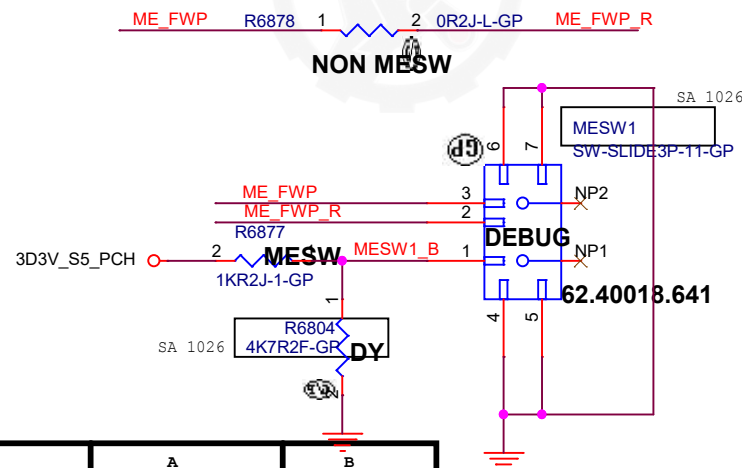
18,24 ESPI\_IO[3..0]  
ESPI\_IO3  
ESPI\_IO1  
ESPI\_IO2  
ESPI\_IO0

24 ME\_FWP  
19 ME\_FWP\_R

## Debug Connector



## Firmware SW



	A	B
ME_FWP_R	Low	High
	Normal Operation (Default)	Override

MESW1\_B  
ME\_FWP\_R  
ME\_FWP  
AFTP6801 AFTE14P-GP  
AFTP6802 AFTE14P-GP  
AFTP6803 AFTE14P-GP

BOLT 15 32bit 0822



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Dubug connector**

Size  
A4

Document Number

**BOLT WHL**

Rev


**A00**

Date: Thursday, December 27, 2018

Sheet 68 of 106

(Blanking)

BOLT 15 32bit 0822

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Title			
<b>Reserved</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
Date: Thursday, December 27, 2018		Sheet 69 of	105

Main Func = Free Fall Sensor

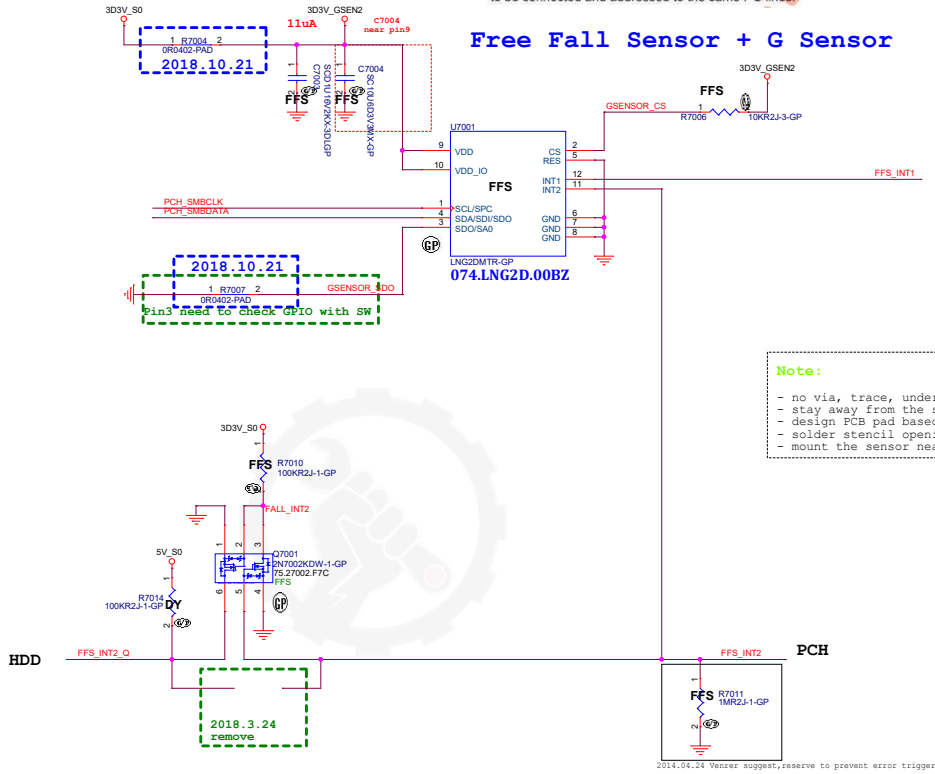
Vinafix.com

The slave address (SAD) associated to the **LNG2DM** is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I<sup>2</sup>C lines.

### Free Fall Sensor + G Sensor

12,13,18,56 PCH\_SMBDATA <<>>  
12,13,18,56,90 PCH\_SMBCLK <<>>

18 FFS\_INT1 <<<<  
20 FFS\_INT2 <<<<  
60 FFS\_INT2\_Q <<<<



**Note:**

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

**Note:**

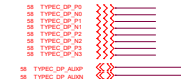
- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

BOLT 15 32bit 0822

From USB HOST



From DP Demux



From CCG4



From CCG4 to MUX & DP Demux



To Type-C CONNECTOR



USB HOST

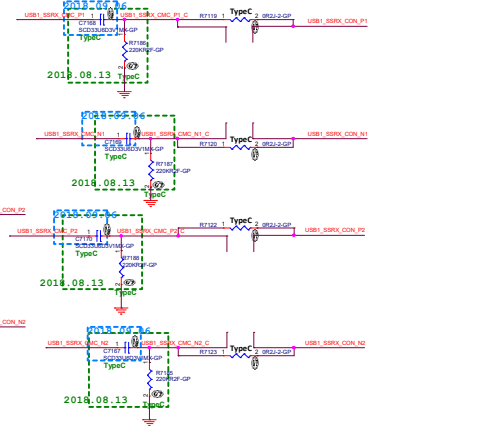
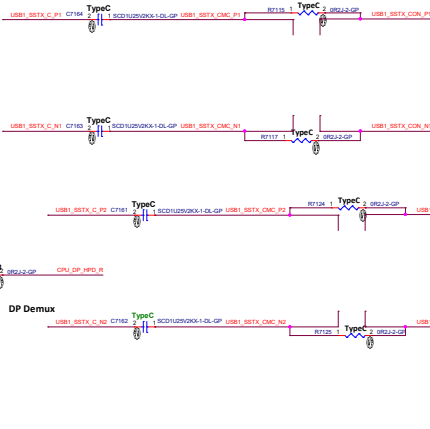
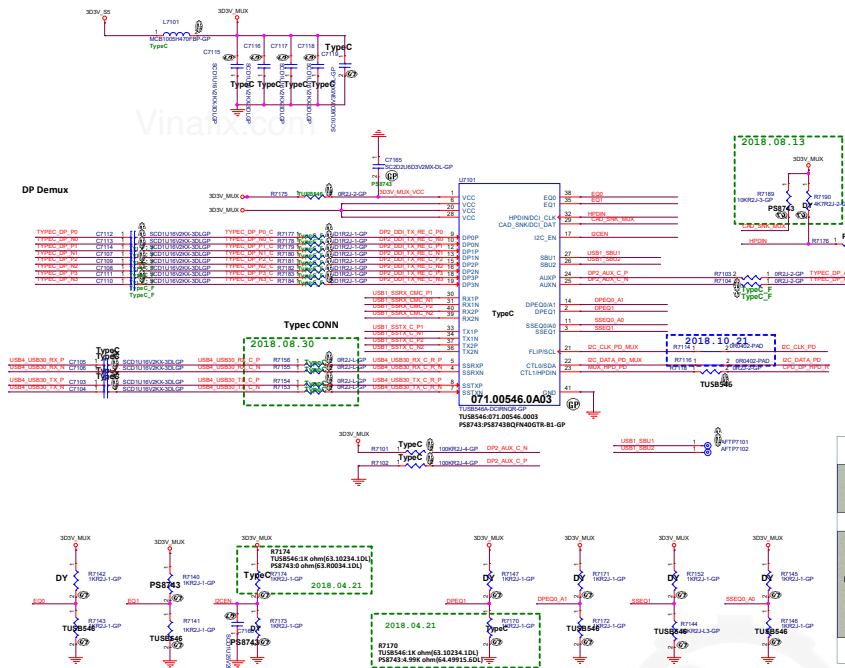
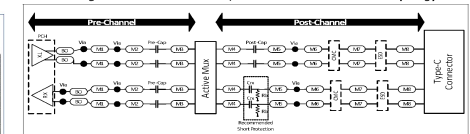
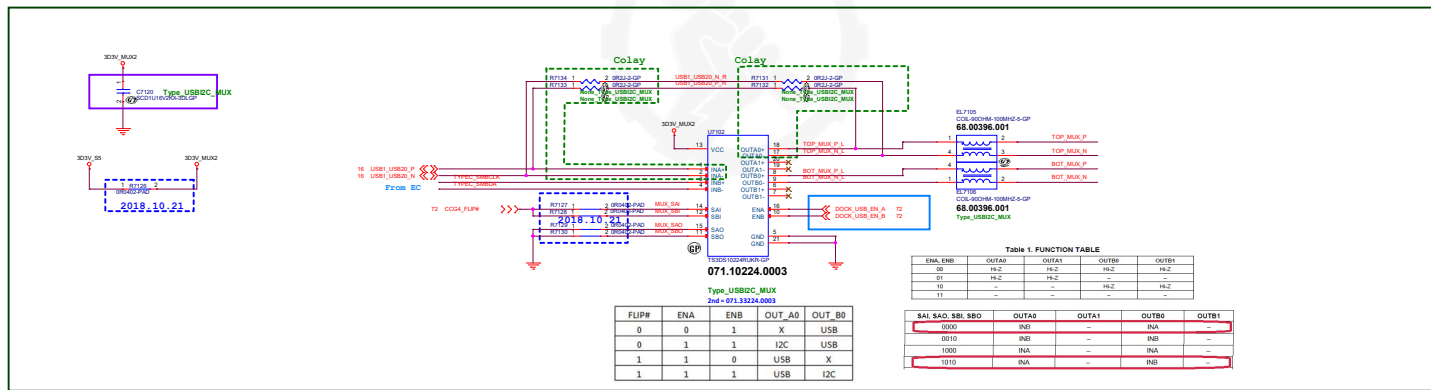


Figure 6-54. USB 3.1 Gen1/Gen2 Active Mux External Topology



Channel	Parameter	Segment	Stackup	Via Count	Gen2	
					Length (mm)	Length (mils)
Pre-channel	Max Trace Length	B0	MS/SL/DSL	1	Note#1*	Note#1*
	Max Trace Length	M1	MS/SL/DSL	1	Note#1*	Note#1*
	Max Trace Length	M2-M3	MS	0	Note#1*	Note#1*
Post-channel	Max Trace Length	M4 + M5	MS	1	7.6	300
	Max Trace Length	M6-M7	M5		7.6	300
	Max Trace Length	M8	M5		10.2	400



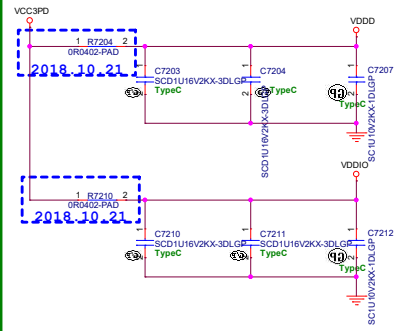
ENB	ENB	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	X	USB
1	1	0	USB	X
1	1	1	USB	I2C

ENB	ENB	ENB	OUT_A0	OUT_B0
00	HL2	HL2	HL2	HL2
01	HL2	HL2	HL2	HL2
11	HL2	HL2	HL2	HL2

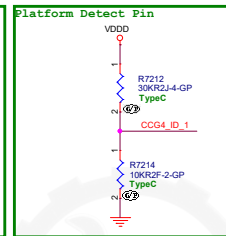
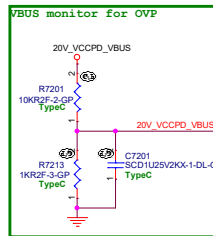
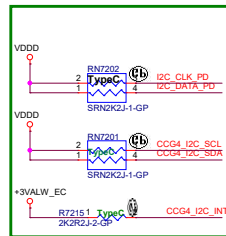
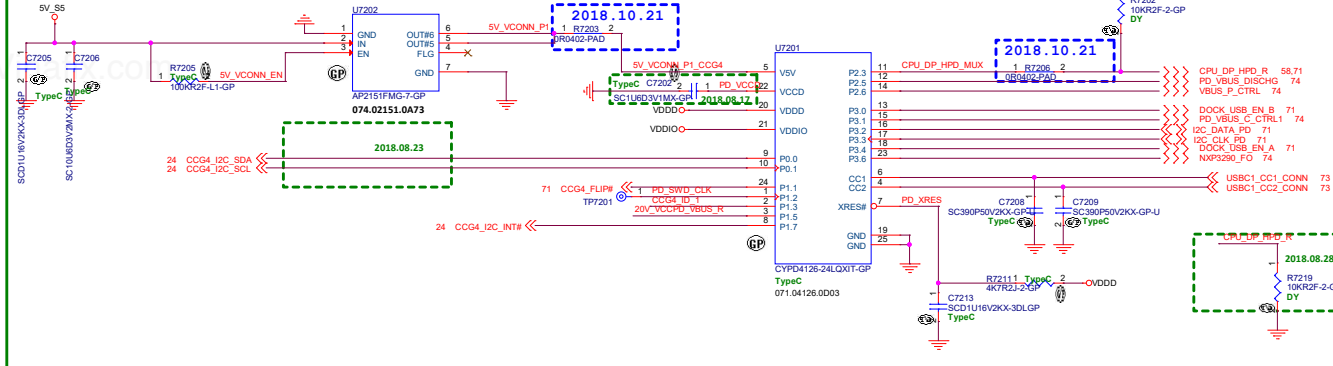


# Main FUNC = CONTROLLER

## Power



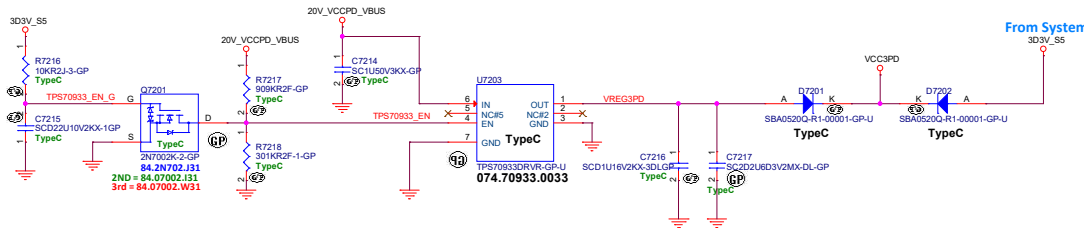
## TYPE C CONTROLLER



CCG4 ID	R7212	R7214	計算値	理論値
0/8	L0	DY	64.10035.6DL (100K)	0
1/8	L1	64.71535.06D1 (715K)	64.10035.6DL (100K)	0.123
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5
5/8	L5	64.12035.6DL (120K)	64.20035.6DL (200K)	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728
7/8	L7	64.10035.6DL (100K)	64.71535.06D1 (715K)	0.877

S.No	Project Name	ODM	CCG4 ID	Single/ Dual Port	Port 1 Configuration	Port 2 Configuration	Voltage level	Voltage value
1	Bolt (VHL) Data Only with PS8743B Max	Wistron	L0	Single	USB	N/A	1.0	0V
2	Bolt (VHL) Data Only with TUSB546 Max	Wistron	L1	Single	USB	N/A	1.1	3.3V/8
3	Bolt (CNL) Data Only with PS8743B Max	Wistron	L2	Single	USB	N/A	1.2	2 * 3.3V/8
4	Bolt (CNL) Data Only with TUSB546 Max	Wistron	L3	Single	USB	N/A	1.3	3 * 3.3V/8
5	Bolt (VHL) Full Feature with PS8743B Max	Wistron	L4	Single	USB+DP+ PD Charging	N/A	1.4	4 * 3.3V/8
6	Bolt (VHL) Full Feature with TUSB546 Max	Wistron	L5	Single	USB+DP+ PD Charging	N/A	1.5	5 * 3.3V/8
7	Bolt (CNL) Full Feature with PS8743B Max	Wistron	L6	Single	USB+DP+ PD Charging	N/A	1.6	6 * 3.3V/8
8	Bolt (CNL) Full Feature with TUSB546 Max	Wistron	L7	Single	USB+DP+ PD Charging	N/A	1.7	7 * 3.3V/8

## For Dead Battery modify

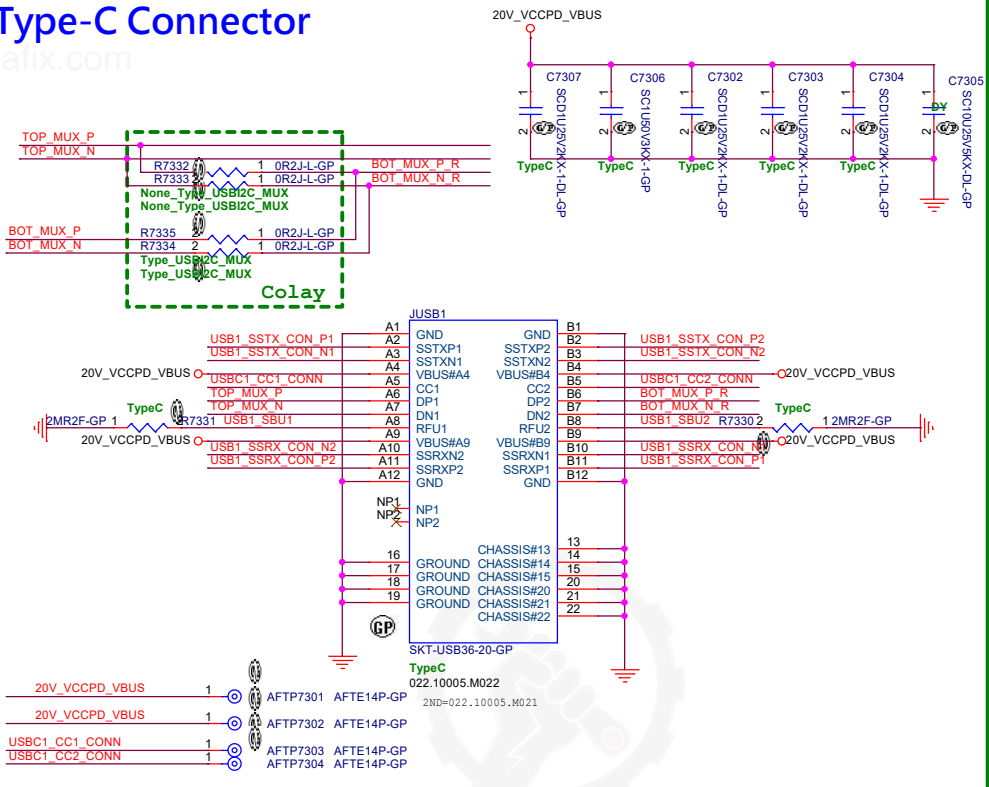


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<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 8th, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.		Title	
Size		Document Number	
Custom		BOLT WHL	
Date: Thursday, December 27, 2018		Sheet 72 of 105	

Main FUNC = TYPEC CONNECTOR

Type-C Connector

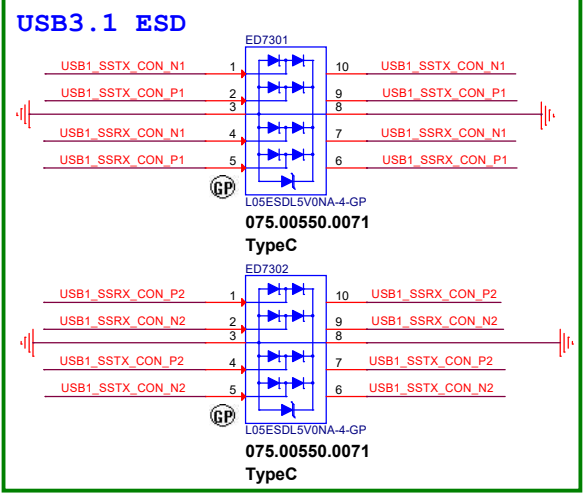
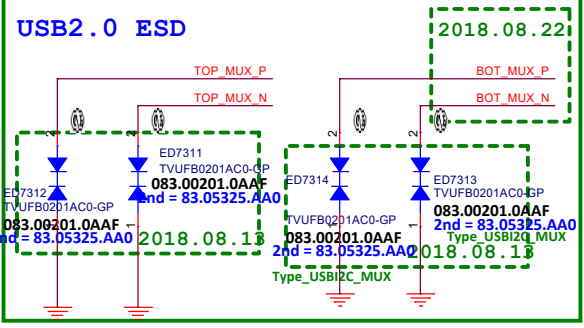
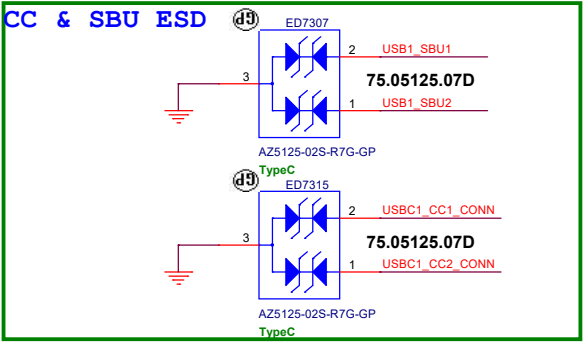


71 USB1\_SSRX\_CON\_N1 <<<<  
71 USB1\_SSRX\_CON\_P1 <<<<  
71 USB1\_SSRX\_CON\_N2 <<<<  
71 USB1\_SSRX\_CON\_P2 <<<<  
71 USB1\_SSTX\_CON\_N1 >>>>  
71 USB1\_SSTX\_CON\_P1 >>>>  
71 USB1\_SSTX\_CON\_N2 >>>>  
71 USB1\_SSTX\_CON\_P2 >>>>

71 USB1\_SBU1 >>>>  
71 USB1\_SBU2 >>>>  
72 USBC1\_CC1\_CONN >>>>  
72 USBC1\_CC2\_CONN >>>>

From USB2.0/ I2C Mux

71 TOP\_MUX\_P <<<<  
71 TOP\_MUX\_N <<<<  
71 BOT\_MUX\_P <<<<  
71 BOT\_MUX\_N <<<<



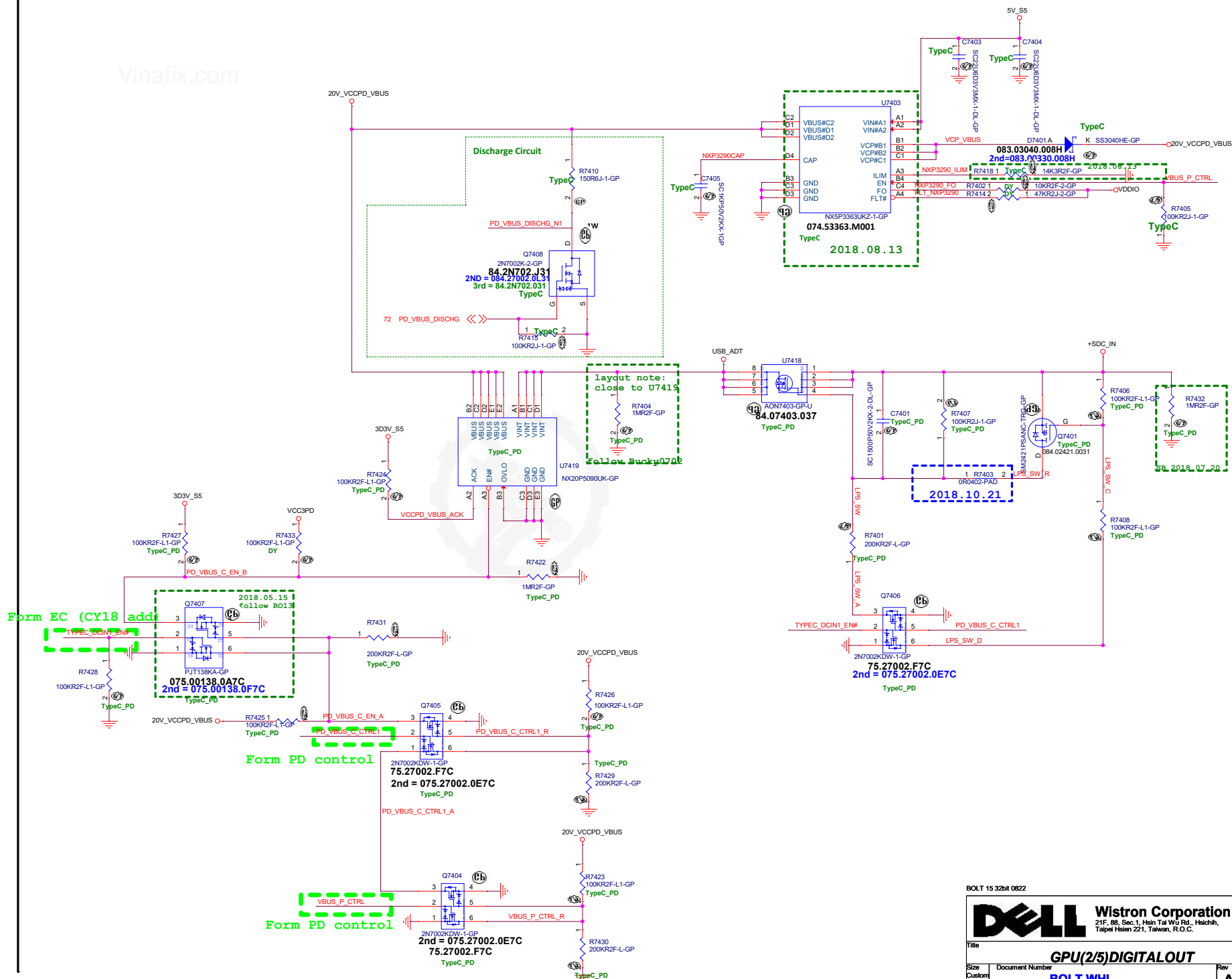
**Main FUNC = LPS**

```

72 PD_VBUS_C_CTRL1 >>>_____
72,74 VBUS_P_CTRL >>>_____
24 TYPEC_DCIN1_EN# >>>_____
72 NXP3290_FO <<<_____
72,74 VBUS_P_CTRL >>>_____

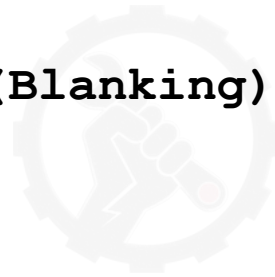
```

44 VCCPD VBUS ACK >>



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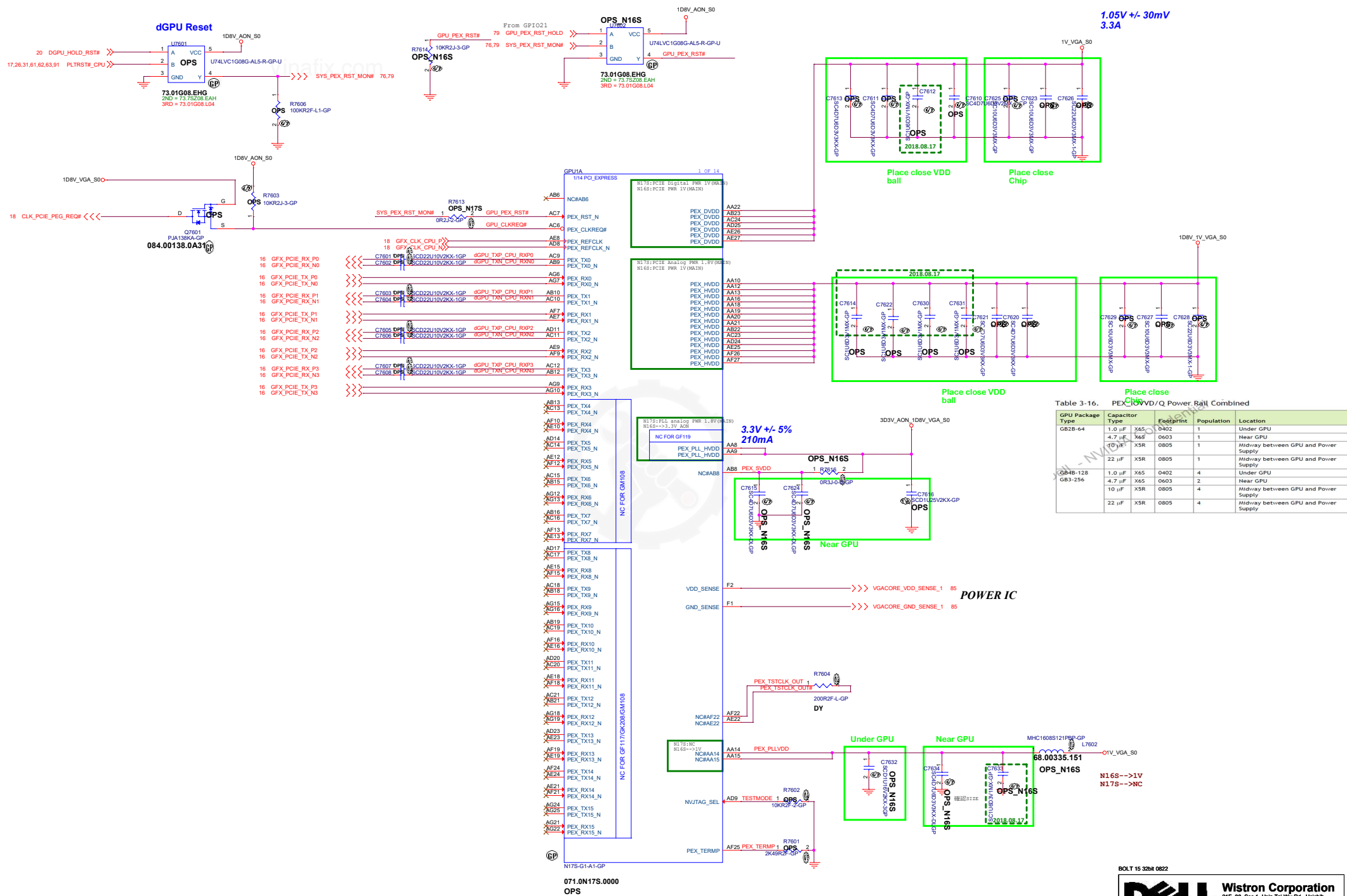
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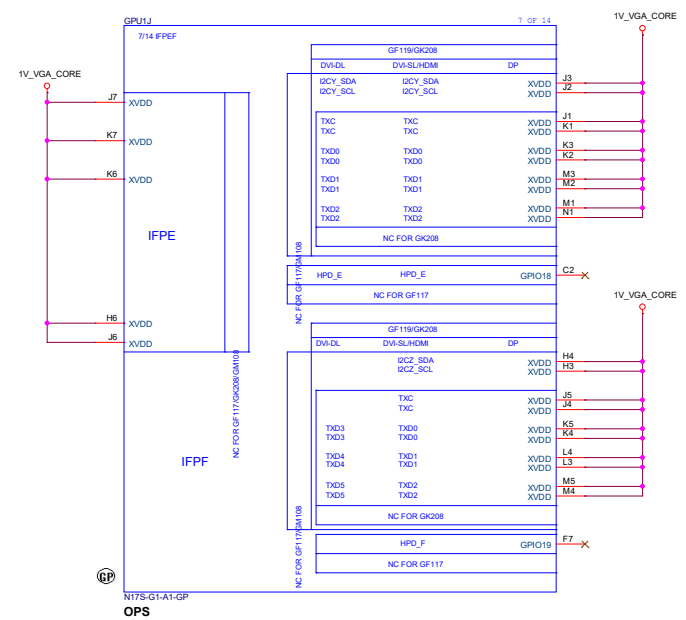
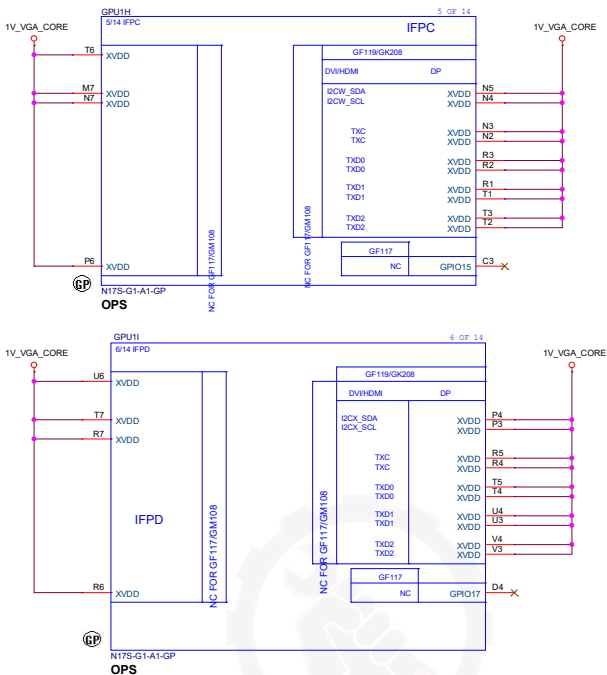
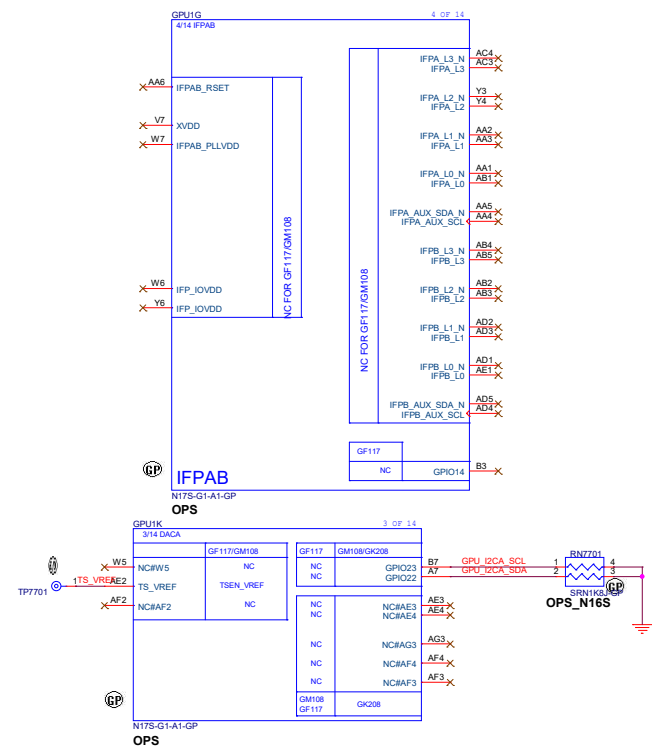
BOLT 15 32bit 0822



Title		
GPU(3/5)VRAM/F		
Size	Document Number	Rev
A3	BOLT WHL	A00
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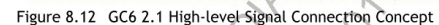


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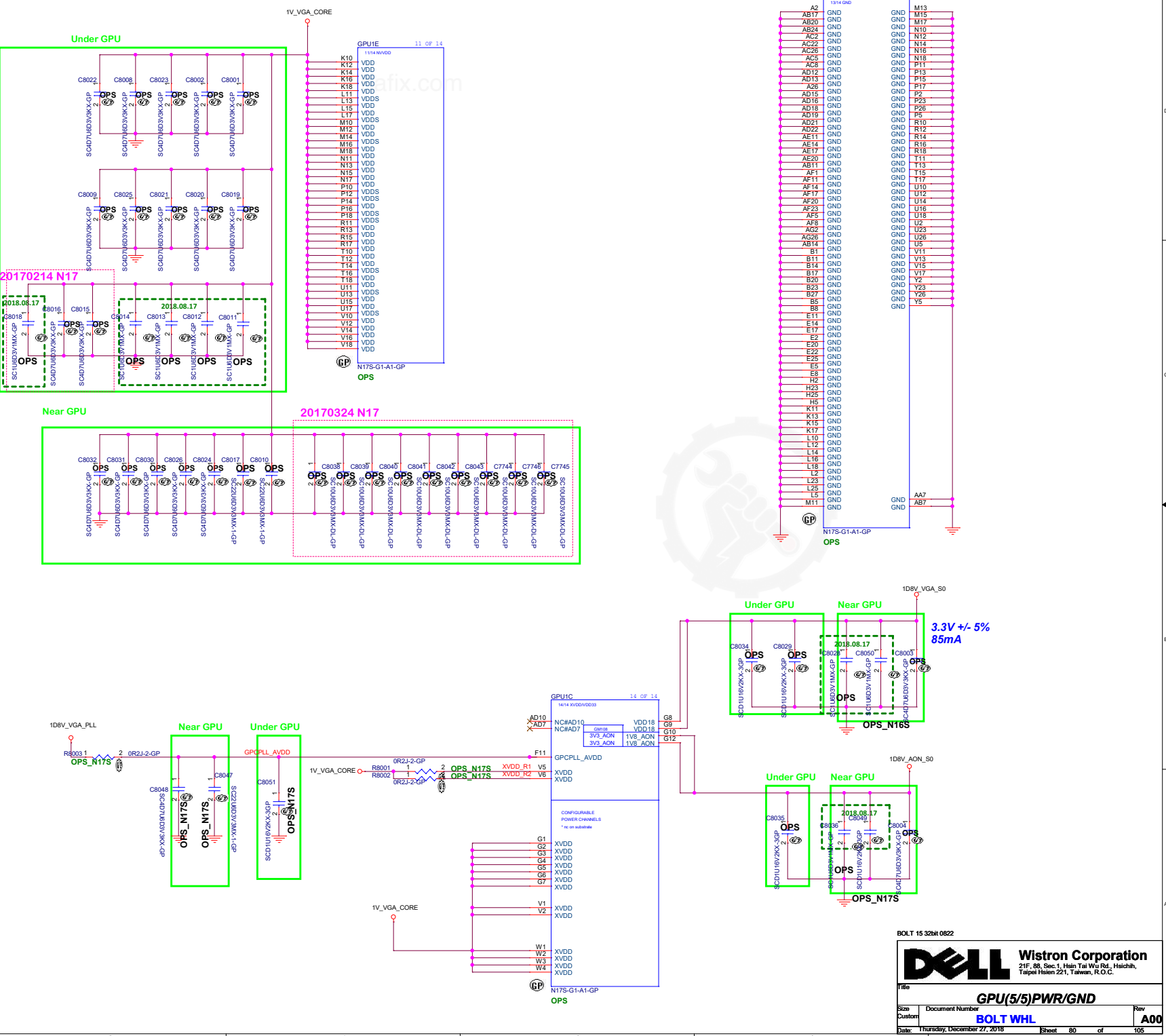
Memory Type	FVFDU/FVFDQ	Memory Density	Manufacturer Part Number	Die Orientation	Package	Speed (MHz)	Date Code Range	Status
Samsung	K4G032M08B-HC-25	8-Mbit	B4E	Down	TSOP	3270	N/A	Production ready
Hynix	H5GC8B46LR-12C	8-Mbit	DS	Up	SO8	2500	N/A	Post production ready
Hynix	H5GC8B46LR-RJC	8-Mbit	DS	Up	SO8	2500	N/A	Substitution allowed with wafer
Hynix	H5GC8B46LR-BJC	8-Mbit	DS	Up	SO8	2000	N/A	Substitution allowed with wafer
Micron	H5T1J2S6A02ZF-40A	A-die	DS1	Down	SO8	3000	N/A	Production ready
Micron	H5T1J2S6A02ZF-70A	A-die	DS1	Down	SO8	3000	N/A	Production ready
Micron	H5T1J2S6A02ZF-S0A	A-die	DS1	Down	SO8	3000	N/A	Substitution allowed with wafer
Micron	H5T1J2S6A02ZF-K0A	A-die	DS1	Down	SO8	3000	N/A	Substitution allowed with wafer
Hynix	H5GC8B46LR-12C	8-Mbit	DS	Up	SO8	2500	N/A	Production ready
Hynix	H5GC8B46LR-RJC	8-Mbit	DS	Up	SO8	2500	N/A	Substitution allowed with wafer
Hynix	H5GC8B46LR-BJC	8-Mbit	DS	Up	SO8	2000	N/A	Substitution allowed with wafer
Samsung	K4G032M08B-HC-25	8-Mbit	B4E	Down	TSOP	3270	N/A	Production ready
Samsung	K4G032M08B-HC-25	8-Mbit	B4E	Down	TSOP	3270	N/A	Substitution allowed with wafer
Samsung	K4G0393M08B-HC-25	8-Mbit	DS	Down	TSOP	3270	N/A	Substitution allowed with wafer
Hynix	H5GC8B46LR-12C	8-Mbit	DS	Up	SO8	2500	N/A	Post production ready
Hynix	H5GC8B46LR-RJC	8-Mbit	DS	Up	SO8	2500	N/A	Substitution allowed with wafer

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<b>GPU(4/5)GPIO/STRAP</b>			
File			
Size Custom	Document Number	<b>BOLT WHL</b>	
Value	1783026, 1783027	2/2	106



Main Func = dGPU



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Taichung Hsien 221, Taiwan, R.O.C.

File: **GPU(5/5)PWR/GND**

Size: Custom Document Number: **BOLT WHL** Rev: **A00**

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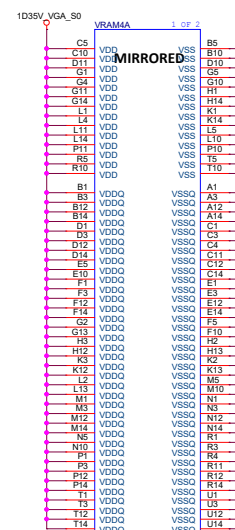
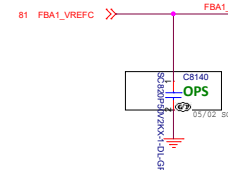
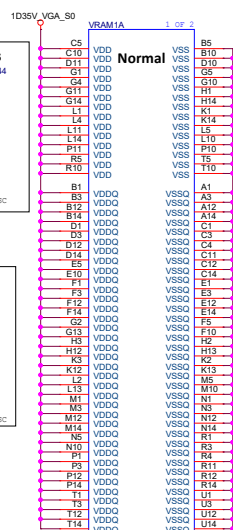
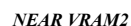
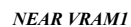
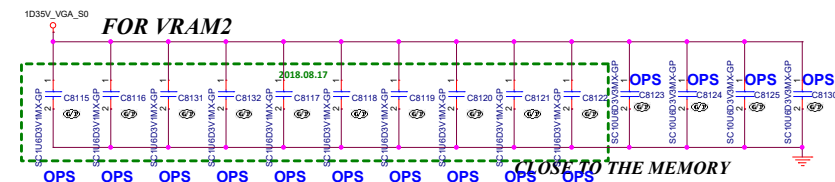
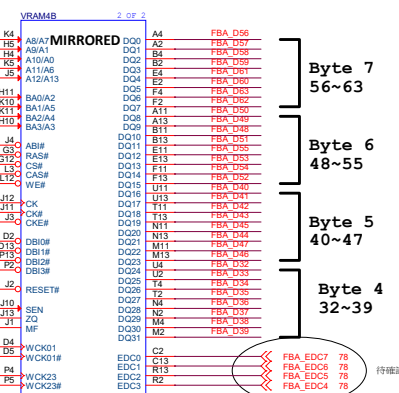
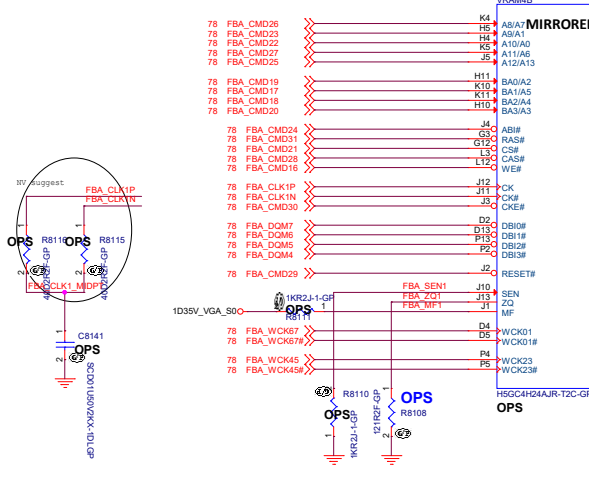
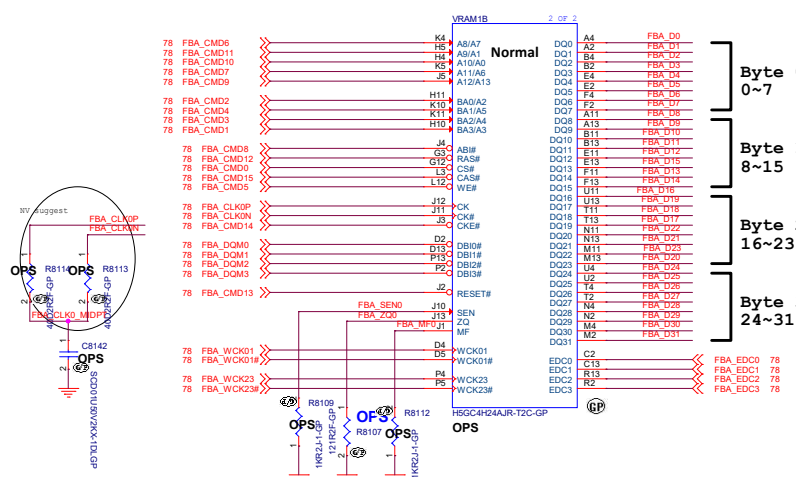


TABLE GDDR5 VIDEO MEMORY		
072.05424.0A0U	072.44132.000U	072.04032.000N

	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)	Micron 4GBITS (128Mx32)
VRAM1 VRAM2	H5GC424AJR-T2C	K4G41325FC-HC03	EDW4032BABG-60-F-0



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BOLT 15 32bit 0622



Title		GPU-VRAM3.4 (2/4)	
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A2	BOLT WHL	A00	
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<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU-VRAM5,6 (3/4)</b>			
Size A3	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU-VRAM7,8 (4/4)</b>			
Size	Document Number		Rev
A3	<b>BOLT WHL</b>		<b>A00</b>
Date:	Thursday, December 27, 2018		Sheet 84 of 105

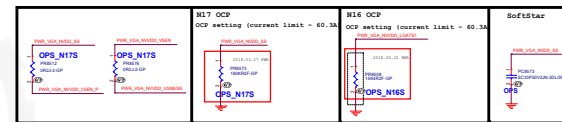
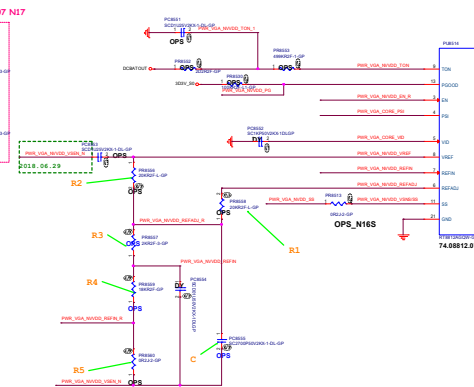
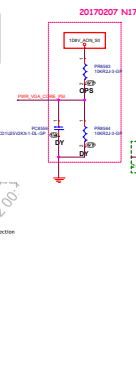
## RT8812A/RT8816A For NVVDD

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Operation Phase Number	PSI Voltage Setting
1 (Phase with DEM)	0.7V to 0.8V
2 (Phase with DEM)	0.7V to 0.8V
3 (Phase with DEM)	1.05V to 1.35V
4 (Phase with DEM)	1.0V to 0.9V

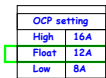
Figure 8-8 GCS 3.1 Voltage Regulator Compensation Signal Connection

Item	Location	N16	N17
1	RT8812A	RT8812A	RT8812A
2	RT8812A	RT8812A	RT8812A
3	RT8812A	RT8812A	RT8812A
4	RT8812A	RT8812A	RT8812A
5	RT8812A	RT8812A	RT8812A
6	RT8812A	RT8812A	RT8812A
7	RT8812A	RT8812A	RT8812A
8	RT8812A	RT8812A	RT8812A
9	RT8812A	RT8812A	RT8812A
10	RT8812A	RT8812A	RT8812A
11	RT8812A	RT8812A	RT8812A
12	RT8812A	RT8812A	RT8812A
13	RT8812A	RT8812A	RT8812A
14	RT8812A	RT8812A	RT8812A
15	RT8812A	RT8812A	RT8812A
16	RT8812A	RT8812A	RT8812A
17	RT8812A	RT8812A	RT8812A
18	RT8812A	RT8812A	RT8812A
19	RT8812A	RT8812A	RT8812A
20	RT8812A	RT8812A	RT8812A

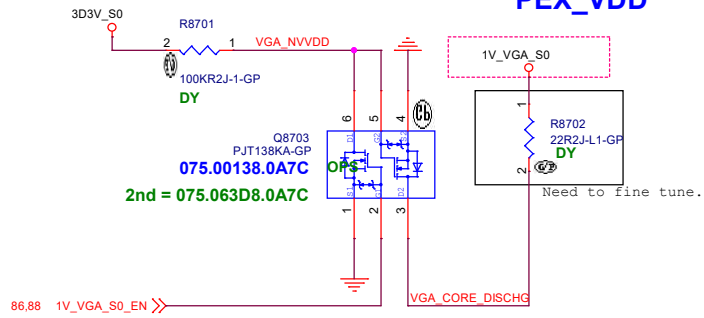




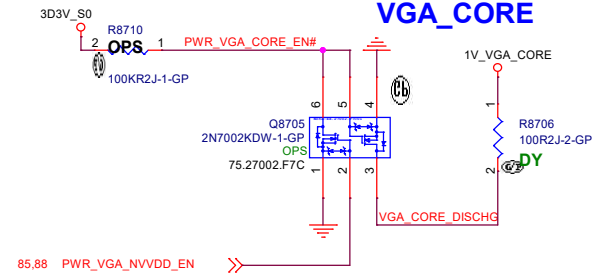
17S(iccmax):0.2A  
17S(icc):0.1A  
16S(iccmax):2.1A  
16S(iccmax):0.8A  
OCP>3A

**SY8288RAC for 1D35V**

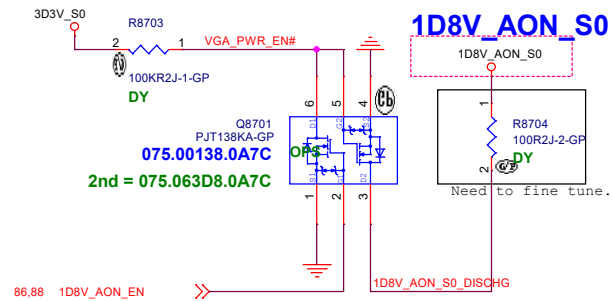
## PEX\_VDD



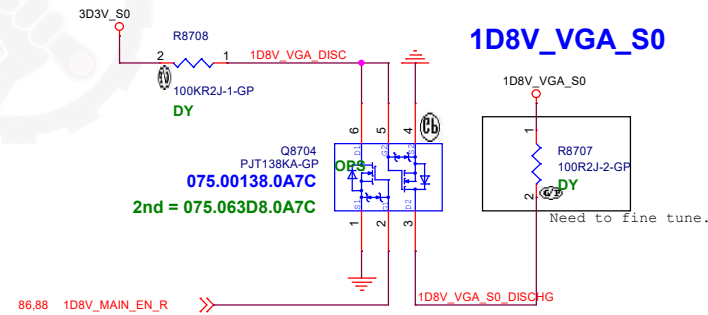
## VGA\_CORE



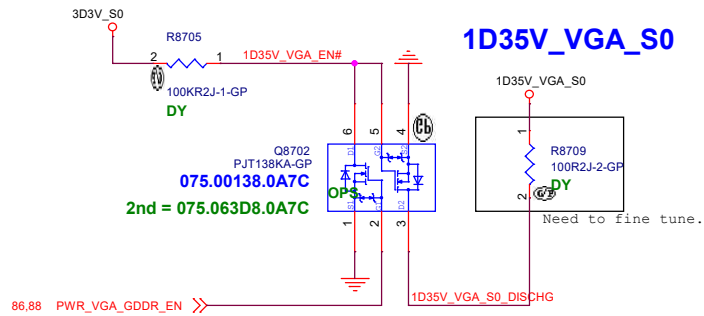
## 1D8V\_AON\_S0



## 1D8V\_VGA\_S0



## 1D35V\_VGA\_S0



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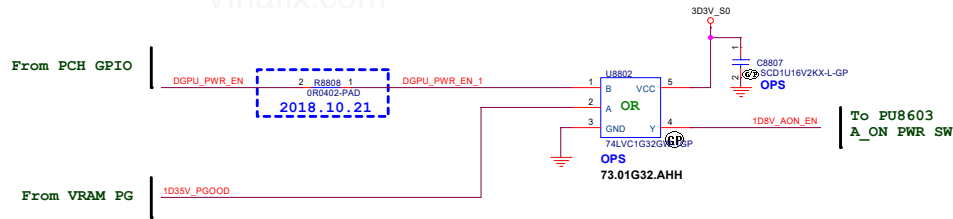
Title			Reserved	
Size	Document Number		Rev	
A3	BOLT WHL		A00	
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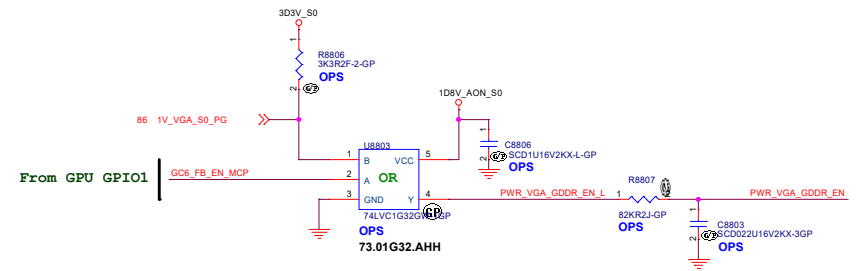
20 DGPU\_PWR\_EN >>>  
85.86 1D35V\_PGOOD >>>  
86.87 1D8V\_AON\_EN <<<  
79 1D8V\_MAIN\_EN >>>  
86.87 1D8V\_MAIN\_EN\_R >>>  
85.87 PWR\_VGA\_NVVDD\_EN <<<

86.87 1V\_VGA\_S0\_EN <<<  
20.79 GC6\_FB\_EN MCP <<<  
86.87 PWR\_VGA\_GDDR\_EN <<<

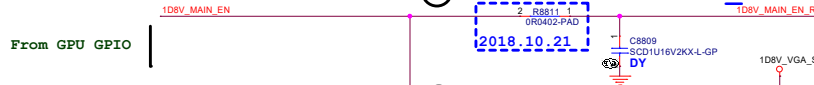
## ① Turn ON/OFF 1V8\_AON



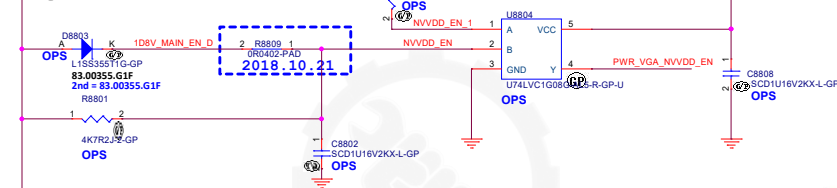
## ⑤ Turn ON/OFF FBVDD



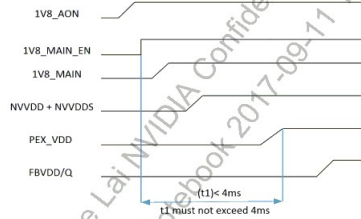
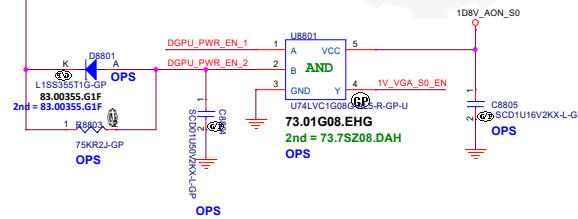
## ② Turn ON/OFF 1D8V\_MAIN



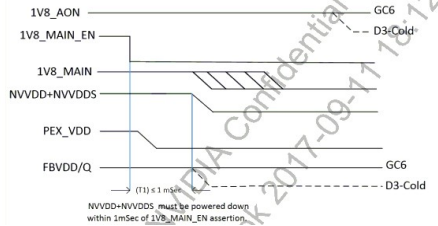
## ③ Turn ON/OFF NVVDD



## ④ Turn ON/OFF PEX\_VDD



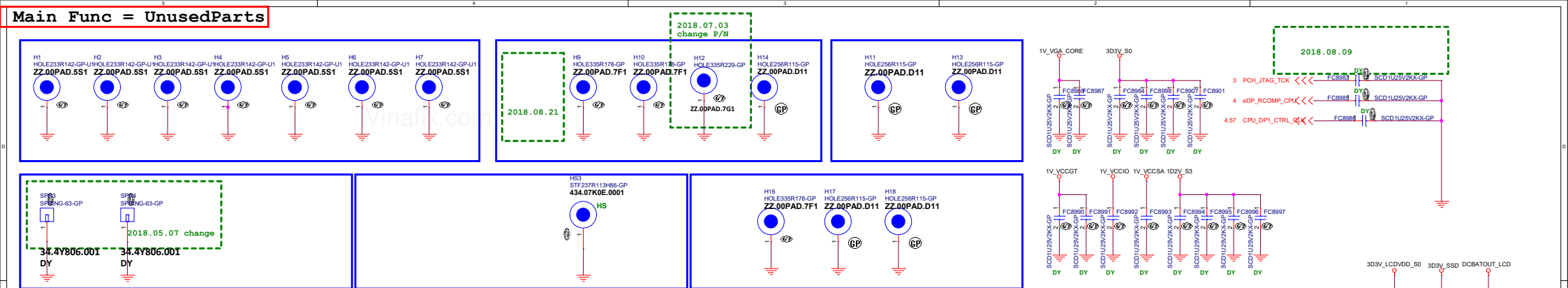
### Power-Down Sequence



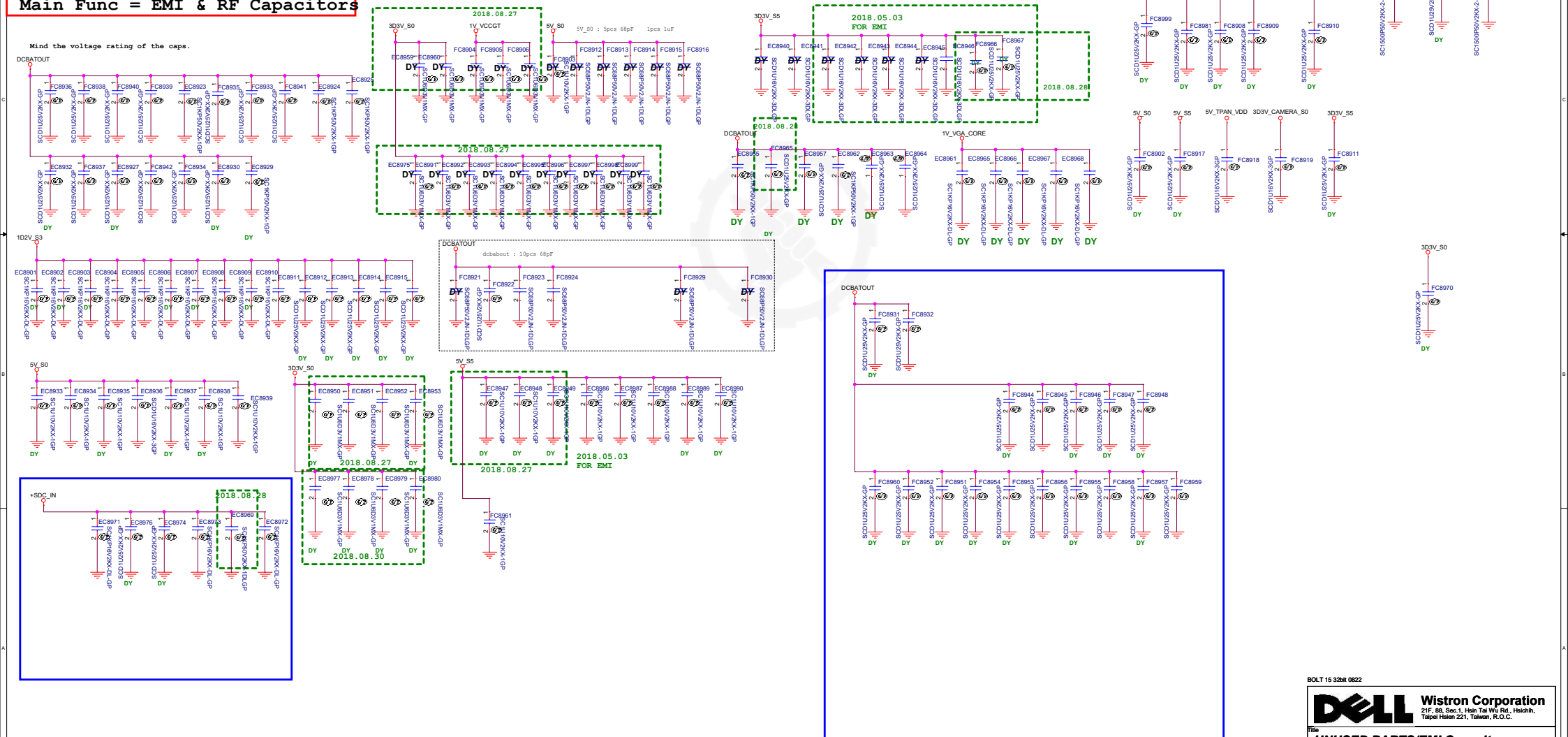
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DELL		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taiwan 300, R.O.C.		GPU SEQUENCE	
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# Main Func = UnusedParts



# Main Func = EMI & RF Capacitors

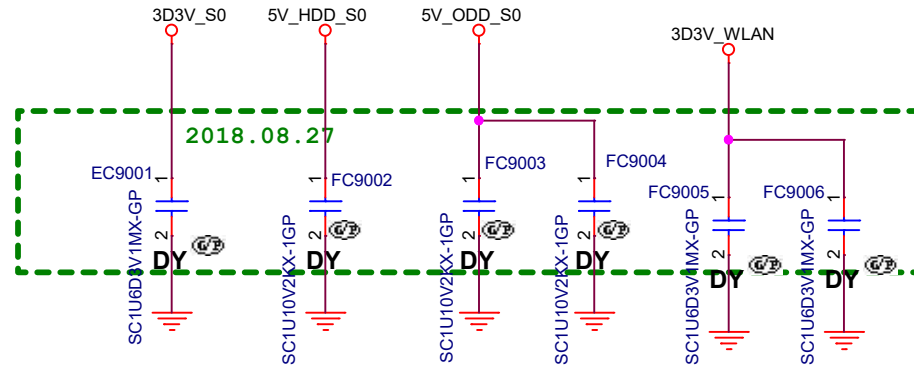


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**DELL** Wistron Corporation  
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Title		
UNUSED PARTS/EMI Capacitors		
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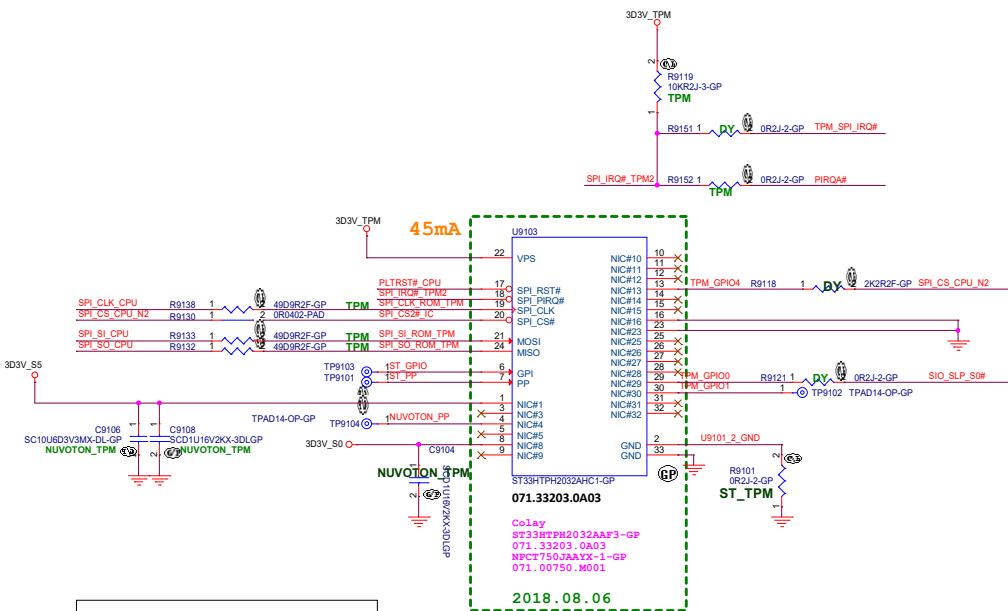
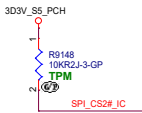
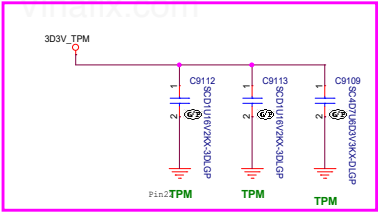


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Title			
<b>Reserved</b>			
Size A4	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
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Main Func = TPM

- 18,25 SPI\_S0\_CPU <<< \_\_\_\_\_
- 18,25 SPI\_CLK\_CPU >>> \_\_\_\_\_
- 15,18,25 SPI\_SI\_CPU >>> \_\_\_\_\_
- 18 SPI\_CS\_CPU\_N2 <<< \_\_\_\_\_
- 17,26,31,61,62,63,76 PLTRST#\_CPU >>> \_\_\_\_\_
- 17,40 SIO\_SLP\_S0# >>> \_\_\_\_\_
- 20 PIRQA# <<< \_\_\_\_\_
- 18 TPM\_SPI\_IRQ# <<< \_\_\_\_\_



R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	DY	DY

BOLT 15 32bit 0822



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Title

TPM2.0

Size

Custom

Document Number

BOLT WHL

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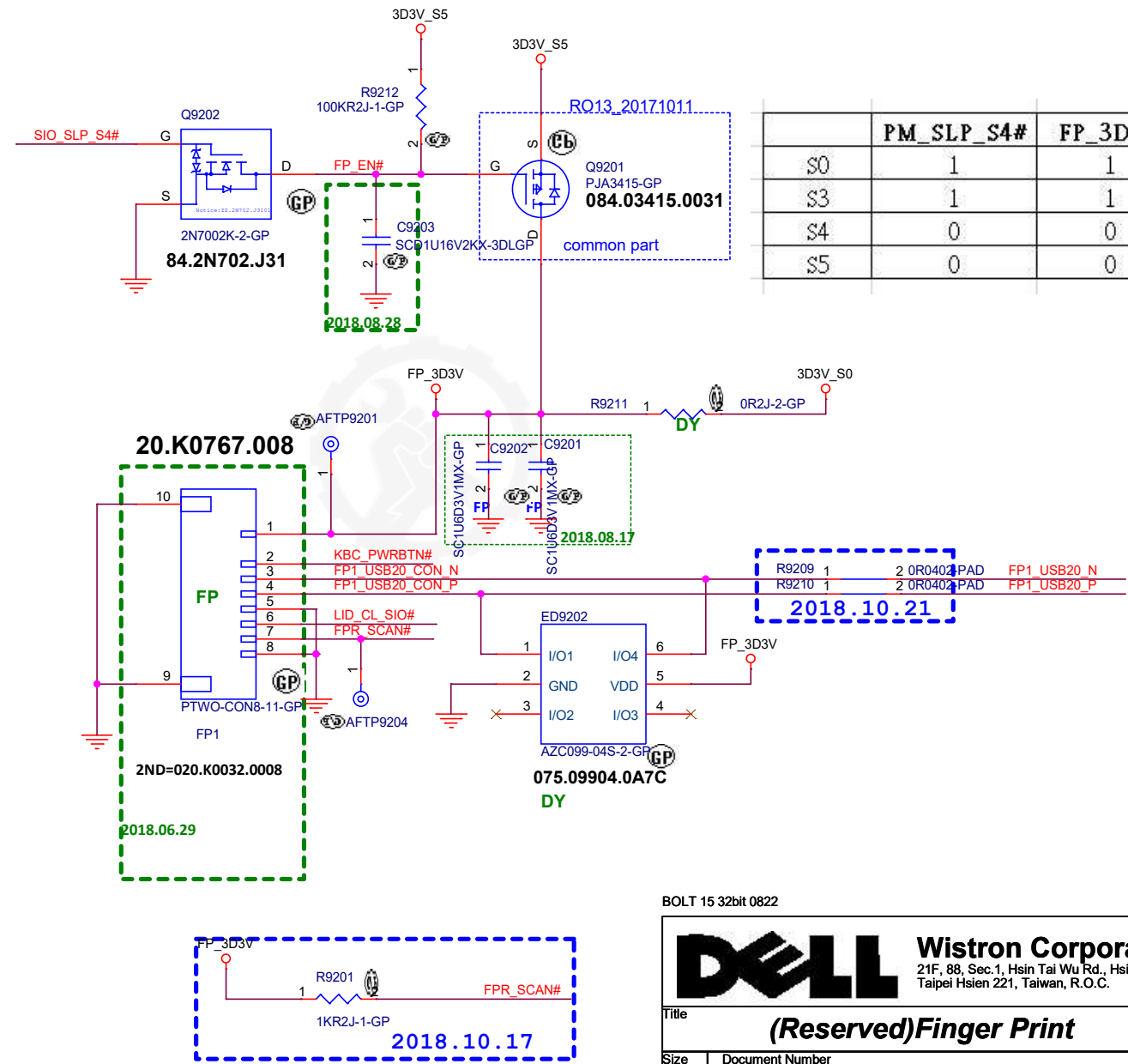
of

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Main FUNC = FPR

Vinafix **FBR(Botton side finger Print Sensor)**

16 FP1\_USB20\_N >>>  
16 FP1\_USB20\_P >>>  
17,40,51 SIO\_SLP\_S4# >>>  
24,64 KBC\_PWRBTN# >>>  
24 FPR\_SCAN# >>>  
24,64 LID\_CL\_SIO# <<<



	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

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Title

(Reserved)Finger Print

Size

Document Number

Rev

Custom

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A00

Date:

Thursday, December 27, 2018

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Title <b>(Reserved)</b>			
Size A3	Document Number <b>BOLT WHL</b>		Rev <b>A00</b>
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BOLT 15 32bit 0822



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Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>(Reserved)</b>		
Size	Document Number				Rev
A3	<b>BOLT WHL</b>				<b>A00</b>
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Title			(Reserved)		
Size	Document Number				Rev
A3	BOLT WHL				A00
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**LVDS\_Switch**

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Size	Document Number		Rev
A4	<b>BOLT WHL</b>		<b>A00</b>
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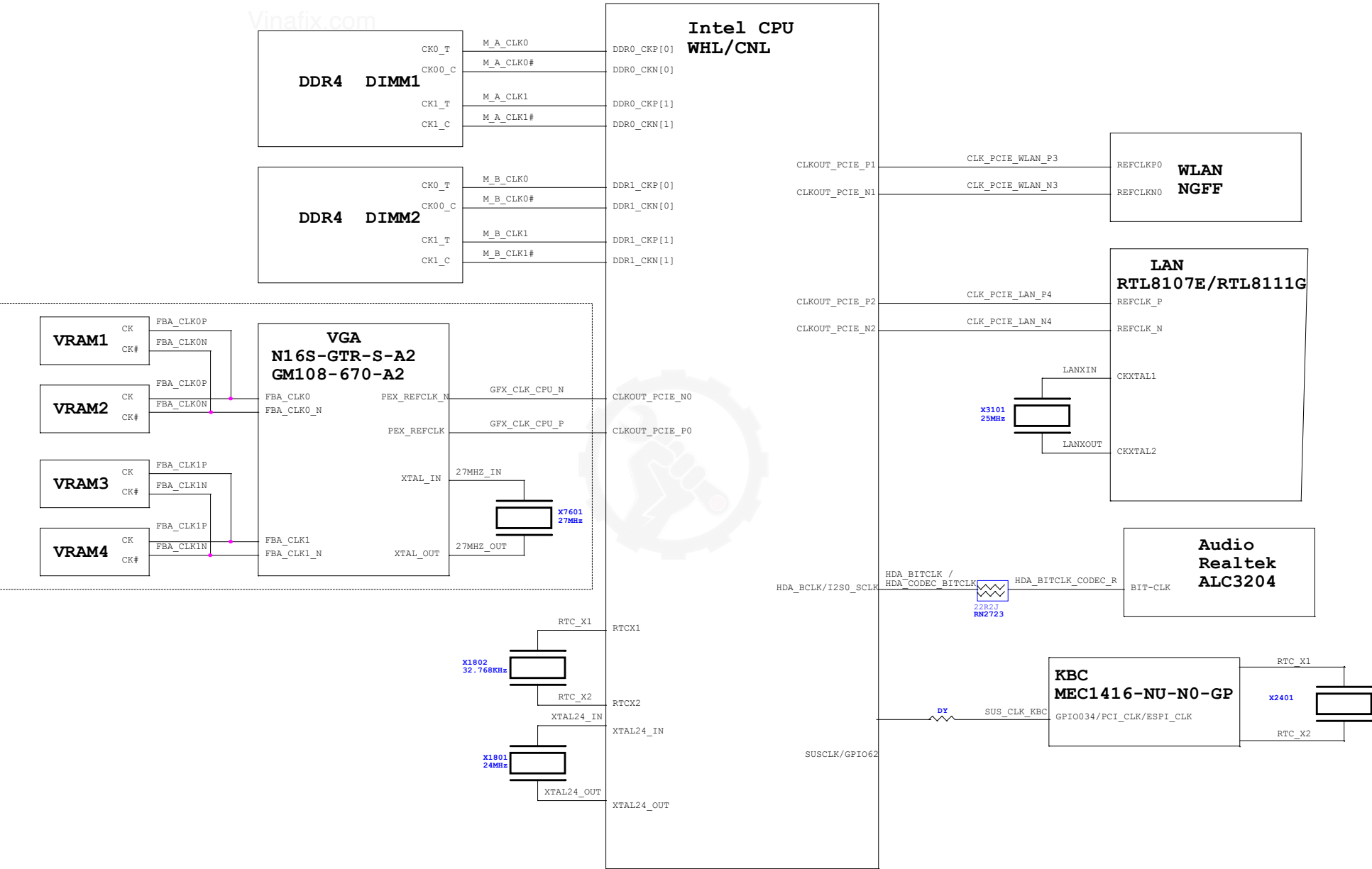
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<b>CPU_XDP:PCH_XDP</b>			
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CLK Block Diagram



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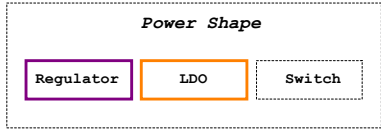
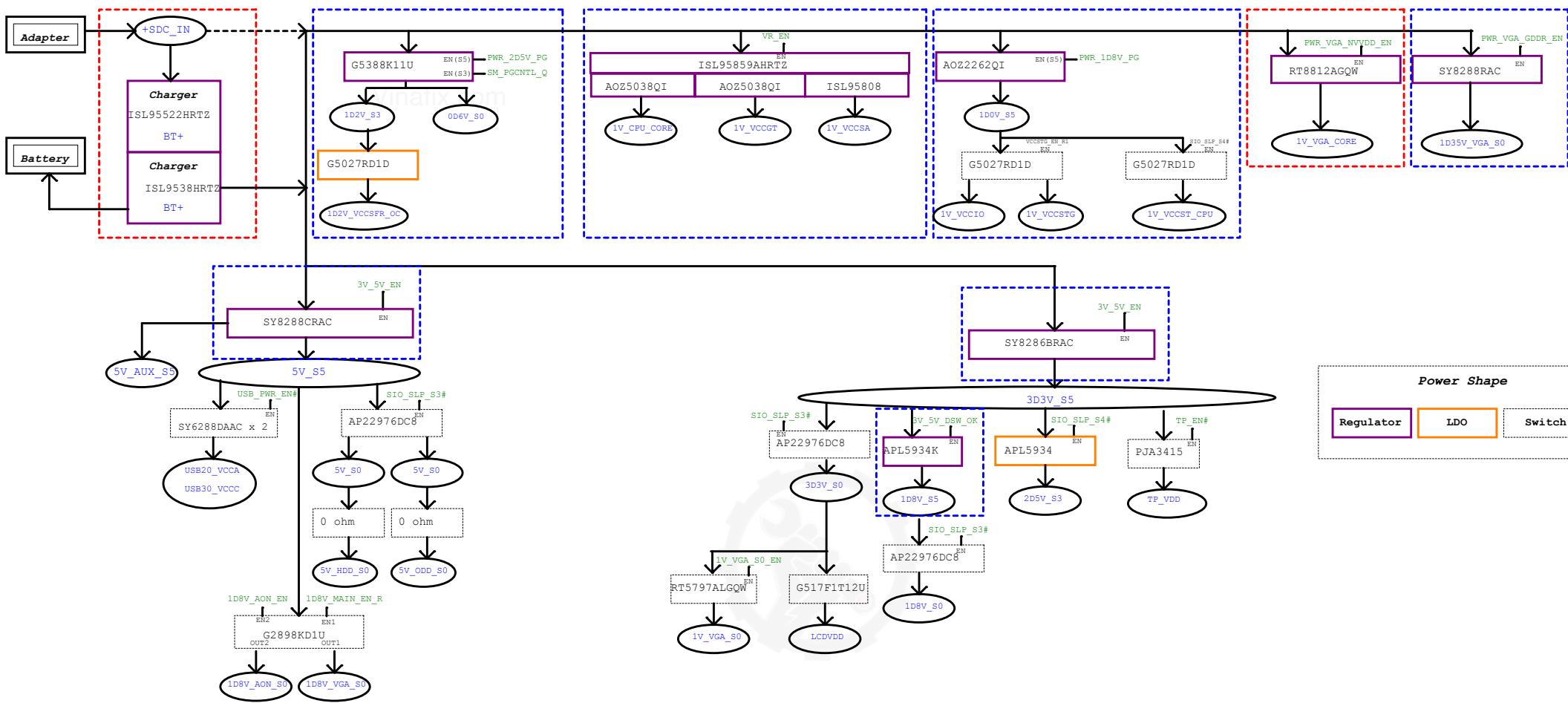
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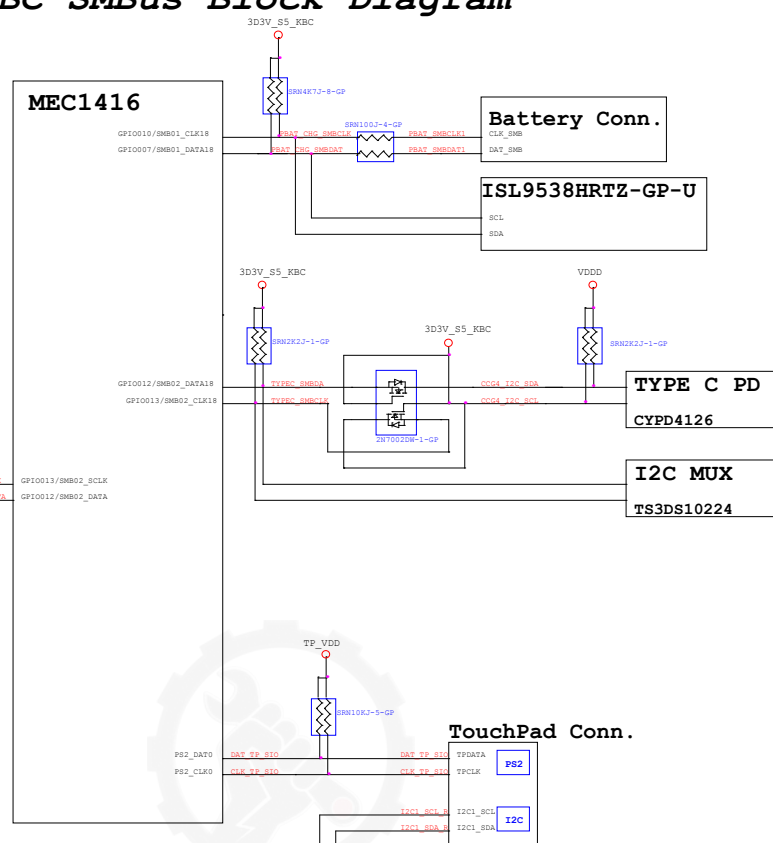
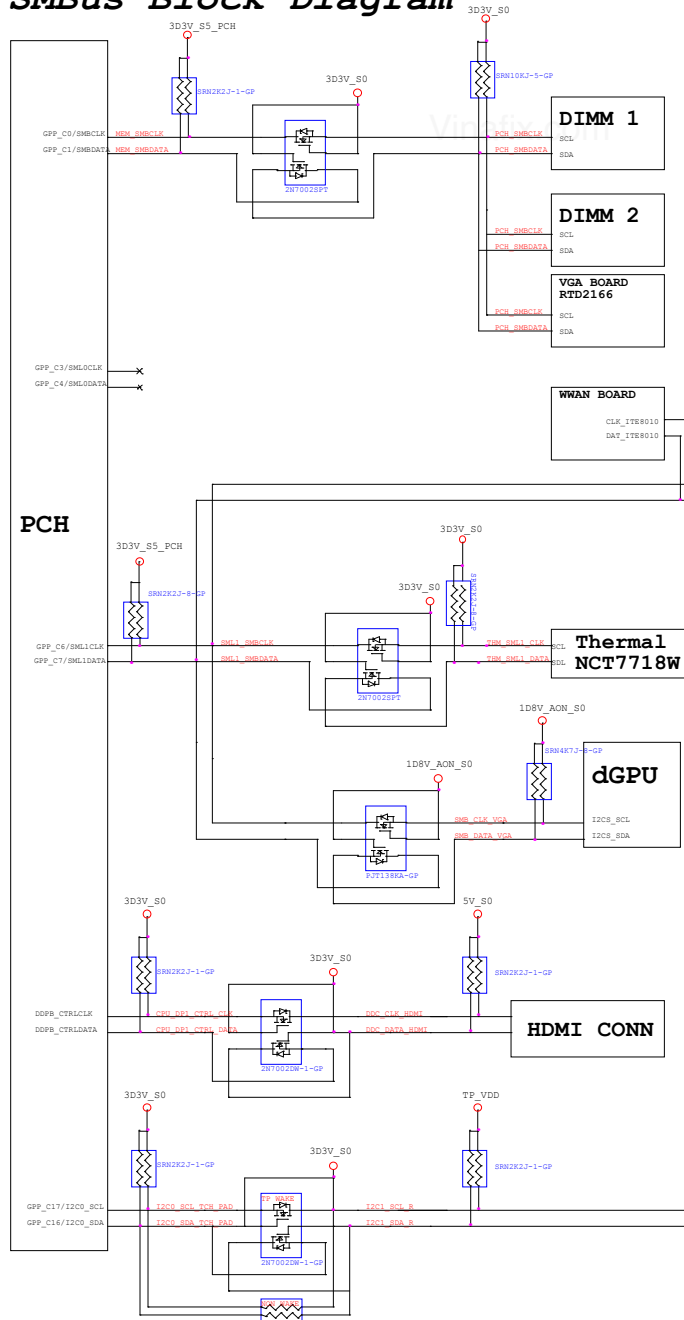
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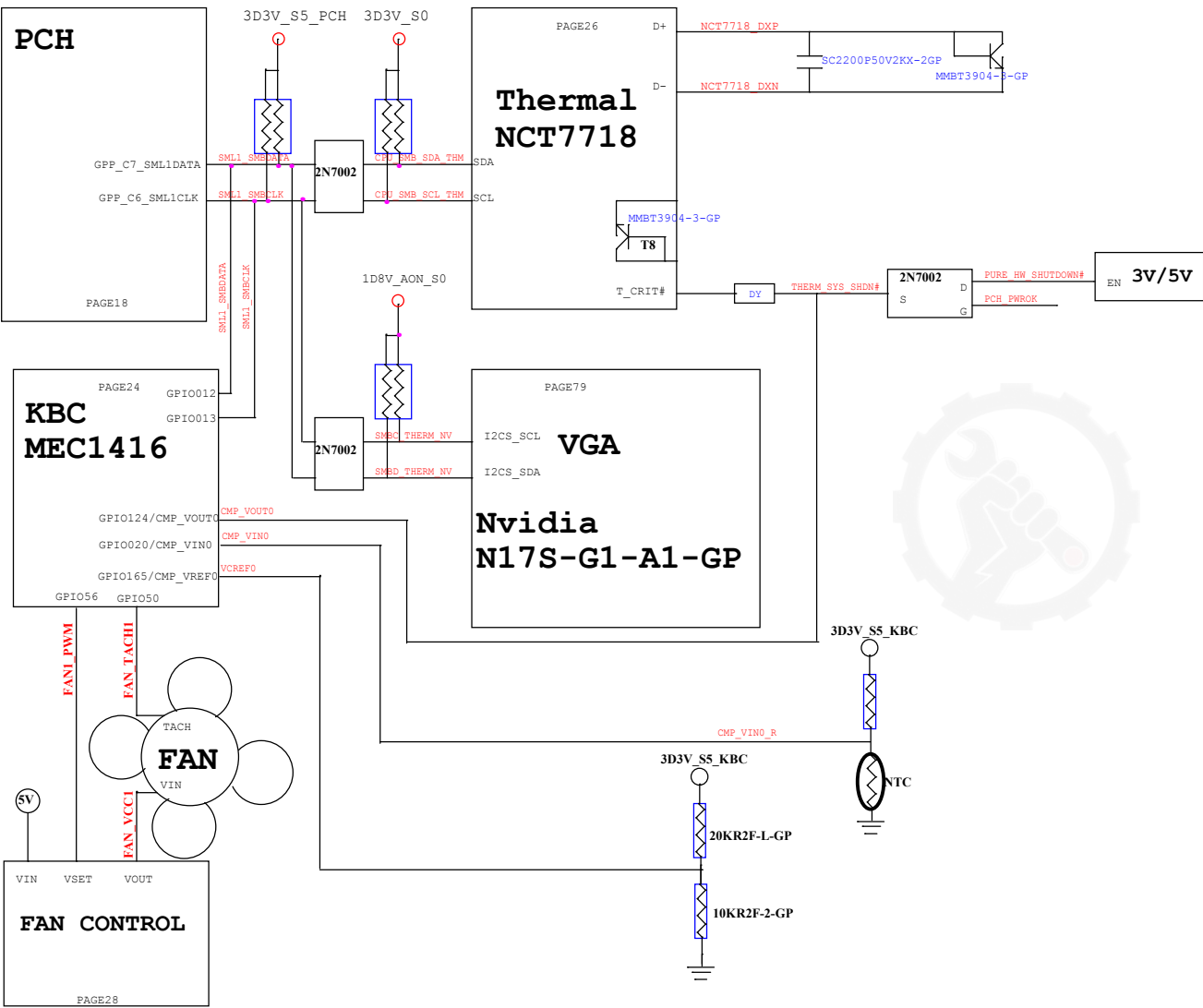


### KBC SMBus Block Diagram



# Thermal Block Diagram

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# Audio Block Diagram

